Designing with the ISL94208 Analog Front End

Description

This application note reviews some of the hardware and software design decisions and shows how to select external components for a multi-cell Li-ion battery pack using a microcontroller and the ISL94208 analog front end.

A microcontroller provides the primary control of the operation of the battery pack. However, the ISL94208 provides several major elements in the multi-cell series Li-ion pack:

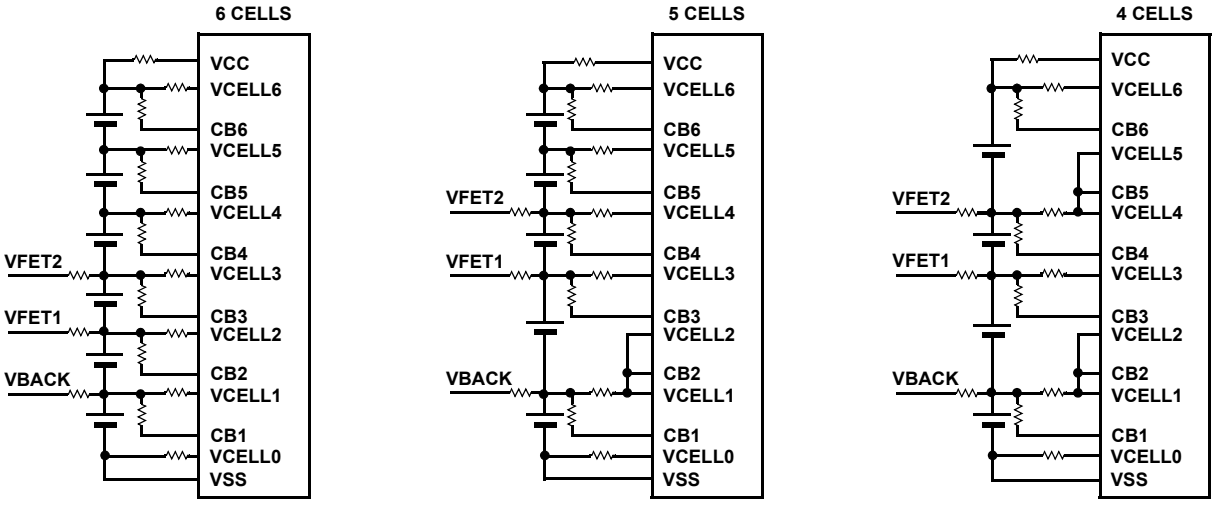
- The voltages involved in a multi-cell series battery pack (up to 26V for 6-cells in series), are far higher than most microcontrollers are rated. So, the ISL94208 provides a voltage regulator supplied from the full battery stack to power the microcontroller. The microcontroller cannot just operate on the voltage from one of the string of Li-ion cells (typically 2.0V to 4.2V each) because higher current from only one cell will cause an imbalance in the battery pack. This will shorten the life of the pack. A later discussion highlights the effects of unbalanced cells and how to rebalance the pack.
- The high voltage of the cells in the pack preclude the microcontroller from directly reading the voltage of each cell as needed to properly manage the charge and discharge limits required of Li-ion cells. So the ISL94208 provides circuits that level shift the voltages across each cell down to a ground referenced voltage that the microcontroller can read using its internal analog to digital (A/D) converter.
- Because the microcontroller is relatively slow to respond to high speed overcurrent events, (such as a short circuit condition) the ISL94208 provides circuits that shut down the pack quickly and autonomously of the microcontroller to protect the cells and the electronics in the pack.
- In order to balance the cells in the pack, the ISL94208 provides the microcontroller the cell balancing circuitry for each cell. Most of these circuits are at a voltage too high for direct microcontroller control.
- To control the current flow into and out of the battery pack, the system typically uses N-channel FETs, one for charge control and one for discharge control. These cannot normally be controlled directly by the microcontroller, because of voltage constraints. Instead, the ISL94208 provides the FET drive circuits.

The ISL94208 supports battery pack configurations consisting of 4- to 6-cells in series and 1-cell or more in parallel.

ISL94208 Cell Connections

Pack Sizes

The ISL94208 supports multiple series connected Li-ion cells. The bottom two inputs and the top two inputs, VCELL1, VCELL2, VCELL5, and VCELL6 are always required. VCELL3 and VCELL4 are optional. This allows the ISL94208 to be used in battery packs of 4- to 6-cells. Simplified connection guidelines for each cell combination are shown in Figure 1.



Note: Multiple cells can be connected in parallel.

FIGURE 1. BATTERY CONNECTION OPTIONS

Connection Recommendations

The ISL94208 was designed for random connection of cells, however, the following are some precautions and recommendations to achieve the best performance.

- The cell input voltage differential VCELLn - VCELL(n-1) should not be forced to greater than the specified limit, as shown in the ISL94208 data sheet. This means, for example, do not connect CELL1 to VCELL1 and CELL3 to VCELL2. It is OK to connect CELL1 to VCELL1 and CELL3 to VCELL3 while VCELL2 is not connected.
- When initially connecting cells to the ISL94208, especially when using a connector where there can be random connection of the voltages, there can be an input surge current large enough to damage the device. To minimize this current and to prevent damage to the device, the best solutions are to reduce or eliminate any input capacitors and add input series resistors. It is not always possible to eliminate capacitors on the input if filtering is needed. In this case, use larger value input resistors. There is a trade-off in this case between hot plug protection, cell balance current, and use of additional external components. For a longer discussion on this topic, see "External Balancing Elements" on page 3.

INPUT CURRENT

Cell voltage measurement occurs when the external microcontroller writes a value to the AO3:AO0 bits. A value of 0 selects no output. A value of 1 through 6 selects CELL1 to CELL6 and places the cell voltage (divided by two) on the AO pin, relative to the VSS ground reference.

The ISL94208 input multiplexer and level shifter mainly use a balanced circuit when the cell voltage is being measured, with identical current into or out of each measured input pin. When the cell is not being measured, there is no VCELLn current.

Table 1 shows typical input currents for the ISL94208 level shifter. In this table, each column shows the cell being monitored (by writing to the AO3:AO0 bits) and the row shows the current into (or out of each cell). A negative value indicates that current is out of an input during measurement.

As shown in Table 1, the currents on most inputs are roughly equal. In this way, equal resistors (even 1kΩ resistors) on both inputs result in little or no voltage measurement error.

INPUT FILTERS

The use of input filters on each cell input as well as on the cell balance inputs (see Figure 2) are optional and if not needed are not recommended, but they can be useful in a number of ways.

- Input filters remove noise generated by motors or EMC events. The input voltages can be filtered in software, but this usually requires a more powerful and expensive controller.
- Input filters protect the device against high voltage transients, during fast FET turn-off (for example).
- The resistor part of the filter can protect against hot plug surge currents (although the capacitor part may create additional surge currents as they may instantaneously charge during cell connections).

TABLE 1. VCELLn INPUT CURRENTS DURING CELL MONITORING

INPUT CURRENT BEING MEASURED	CELL BEING MONITORED (As selected by AO3:AO0)						
	CELL1 (µA)	CELL2 (µA)	CELL3 (µA)	CELL4 (µA)	CELL5 (µA)	CELL6 (µA)	CELL7 (µA)
VCELL6						40	40
VCELL5					40	40	
VCELL4				30	40		
VCELL3			30	30			
VCELL2		-20	30				
VCELL1	-18	-20					
VCELL0	-18						

For VCELL1 to VCELL4, the difference in the VCELLn-VCELL(n-1) measurement currents is ±2µA.
For VCELL5 and VCELL6, the difference in the VCELLn-VCELL(n-1) measurement currents is ±4µA.
(From the Data Sheet.)

Input filters do pose some design challenges. The first challenge, voltage drop across input resistors, is mitigated by the matched input measurement currents of the ISL94208. However, because of variations in the input resistors and the measurement current, the microcontroller may need trim the measurements in-circuit to obtain the best accuracy.

The second major problem arises when using the ISL94208 internal balancing FETs. Since the balancing current passes through the input resistor, a large value resistor limits the balancing current. For example, a 1kΩ input resistor limits the balance current to 3-4mA.

An example circuit using both an input filter and internal balancing FETs is shown in Figure 2. When using an input filter resistor along with the on-chip balancing FETs, consider the power dissipation in the resistors during balance. The input and balance resistors need to be able to handle the cell balance current. This is not a problem with the circuit of Figure 2, because the balance current is relatively low. But if the input resistor and cell balance resistor are both 20Ω, for example, then the power dissipation in both the input and balance resistors would be 200mW. The resistors should be sized correctly to handle this. Also, this dissipation can cause heating and affect the accuracy of the voltage measurement.

Another consideration when using internal balance resistors is the power dissipation on-chip. If balancing more than 90mA, then it is not possible to balance five cells at the same time without exceeding the power dissipation of the ISL94208 package.

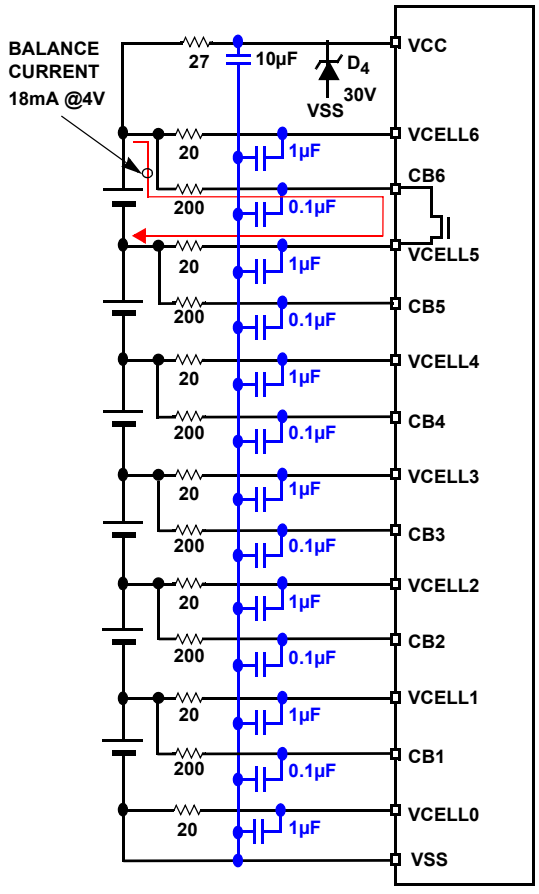
For the VCELL and CB inputs in Figure 2, the values of 20Ω and 200Ω were chosen for the following reasons.

1. A cell balance resistor larger than 200Ω may impose to great a limit on the cell balance current. For example, a 500Ω resistor decreases the balance current to less than 8mA.
2. The input resistor was chosen to be about 10% of the balance resistor. The reason for this is that, when balance turns on, the voltage measured by the ISL94208 drops by the voltage divider created by the CB and Input resistors. A 10% change

in the input voltage is not normally a problem. But, if the CB and input resistors are the same value, then the voltage of the measured cell drops in half during cell balancing. If the microcontroller does nothing, then this condition would likely shut down the power FETs due to a perceived undervoltage condition.

The microcontroller code could ignore the cell voltage during balancing, but if balancing is on for a long time, then ignoring the cell voltage might not be a good choice. Another option for the microcontroller is to turn off balancing during cell measurement, but turning balance on again after measurement requires all conditions be re-verified. This might take too long.

In Figure 2, filters are shown on the cell balance terminals as well as the input terminals. The time constant of the filter on the cell input and the cell balance inputs should match. This is because, with filters only on the VCELLn inputs (or with different time constants), the voltage on the CBn input can greatly exceed the VCELL(n-1) input when the battery cell voltages change rapidly, such as during power FET turnoff during a short circuit. This can result in damage to the internal ESD structure.

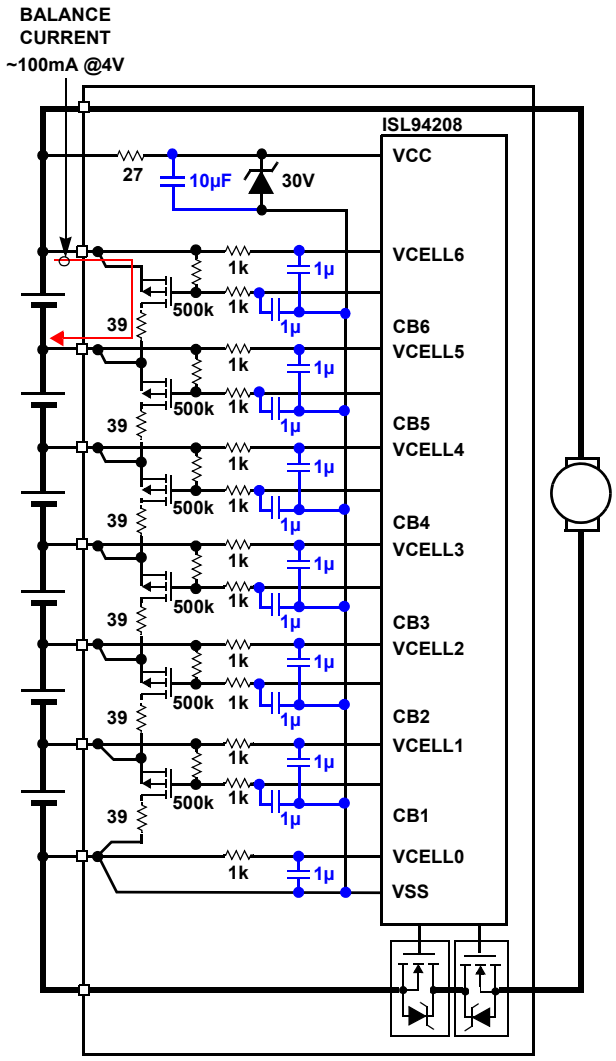


Capacitors (blue) are optional and used when filtering is needed

FIGURE 2. ISL94208 INPUT FILTERS

External Balancing Elements

To allow larger input filter resistors or more filtering, plus provide a high balance current, replace the internal balance FETs with external P-Channel FETs controlled by the CB outputs. These extra FETs add some cost to the system, but they allow very high balancing currents, all cells can be balanced at the same time, the cell voltage measurements during the balance operation are more accurate, and larger input resistors are able to be used to protect against voltage spikes without significantly affecting measurement accuracy.



Capacitors (blue) are optional and used when filtering is needed

FIGURE 3. DIAGRAM OF INPUT FILTER/EXTERNAL P-CHANNEL BALANCING FETS

The connection of input filters and external balancing FETs shown in Figure 3 does have one potential problem. This involves the voltage rating of the P-channel FETs used in the balancing circuit. During a pack short circuit condition, the cell voltages can collapse, due to the high current, and the voltages on the balancing FET's source and drain drop very fast. At the same time, the gate voltage is being held high by the FET gate capacitance. This results in a VGS for the upper balancing FETs that can exceed the normal 20V maximum rating – depending on the various time constants. Adding a diode across the 50k resistor may help prevent this excess gate voltage.

Another potential issue is that the cell balance FET body diode can conduct in a reverse direction when the cell voltages collapse during a pack short circuit. This current can be several hundred mA for a very short time.

See "Cell Balancing" on page 20 for more information about cell balance components and control algorithms.

Voltage Regulator Connection

The ISL94208 can provide 350µA of output current on the RGC pin to drive an external NPN transistor. With a gain of 100 the ISL94208 regulator can supply up to 35mA to an external load, while maintaining the output at 3.3V ±10%. The external transistor should have a V_{CE} of greater than 26V (preferably greater than 35V) for a 6-cell pack.

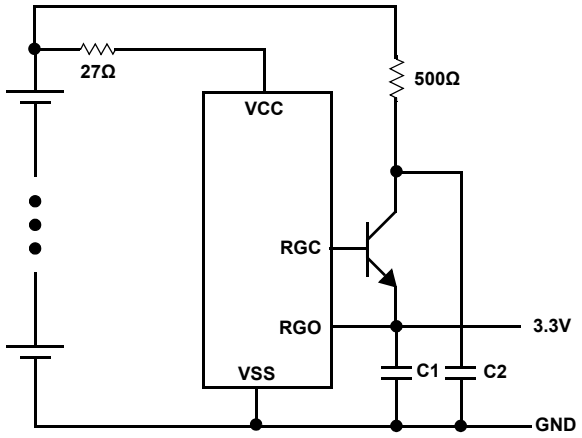


FIGURE 4. VOLTAGE REGULATOR CIRCUIT

A 500Ω resistor is recommended in the collector of the NPN transistor to minimize initial current surge when the regulator turns on. Without the collector resistor, the initial turn-on current surge could be large enough to damage the transistor.

The voltage at the emitter of the NPN transistor is monitored by the ISL94208 and regulated to 3.3V by the control signal at RGC. The RGO voltage also powers many of the ISL94208 internal circuits.

Capacitor C2 in Figure 4 is optional, but can help to minimize noise spikes on the RGO voltage regulator and reduce voltage swings on the supply during initial power-up.

VBACK Connection

The ISL94208 VBACK pin provides a backup supply for the RAM Registers when the RGO regulator turns off. An internal switch detects when the RGO voltage drops too low and automatically switches the supply to VBACK.

VBACK also provides a Power On Reset Circuit. The ISL94208 may power-up/power-down thresholds are based on a pack voltage above 6.5V and the VBACK voltage greater than about 2.05V.

Normally, the VBACK pin is connected to CELL1, however, it could also connect to an external regulator powered by the pack voltage or from an external source.

To prevent inadvertent loss of data during a short circuit or heavy load condition, in which the battery stack voltage drops to near zero, filters can be used on RGO and VBACK to maintain the voltage until the battery stack recovers following the short circuit event.

FET Supply Pins

There are two FET supply pins, VFET1 and VFET2. VFET2 provides the voltage and current for the CFET and DFET gate drives. VFET1 provides biasing for the gate drive circuits. Normally VFET2 would be tied to the CELL3 voltage and VFET1 would be tied to the CELL2 voltage. Each of these can use input filters to maintain the FET drive during glitches on the Cell voltages.

Connecting VFET1 and VFET2 directly to the Cells (through a filter) provides a low cost solution, however there are several drawbacks to this configuration.

- When the charge FET is on, current for the CFET gate passes through the CFET pull up resistor to ground (see Figure 5.) This current from only some of the cells can lead to cell imbalance.

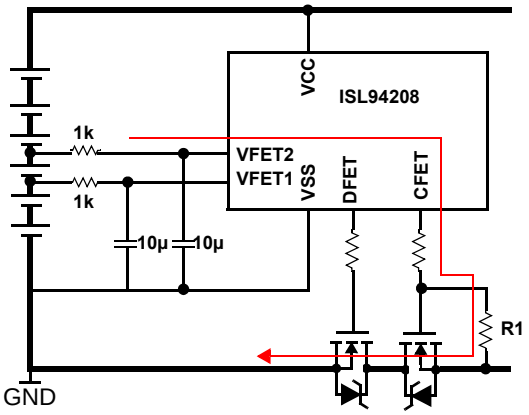


FIGURE 5. BVFET1, VFET2 CONNECTIONS TO CELL VOLTAGES

- The minimum differential between VFET2 and VFET1 for optimal operation of the power FETs is 2.8V. If the cell voltages drop below this level, then the FET control circuit does not have enough headroom to rapidly turn on the FETs. As the voltage drops, the drive capability also drops. At a voltage differential of 2.3V, the ISL94208 does not have the drive capability to keep the FETs on over the full temperature range.

An alternative connection for VFET1 and VFET2 includes a voltage regulator (see Figure 6.) If the designer is concerned that the cells become unbalanced by supplying the FET reference from only one or two cells, then a regulator can be used that is powered by the full stack. In this case, the VFET1 pin needs a supply that is less than VFET2, but not zero. In Figure 6, a 4.3V zener provides the desired reference.

This circuit also solves the second problem related to direct connection of the VFETn pins to the CELLs. By using the external regulator, the pack voltage can drop to 8.6V (or a little below) and still provide adequate FET drive. For a 6-cell pack, this means that the minimum cell voltage is 1.4V per cell. For a 4-cell pack, it is 2.15V per cell.

According to the data sheet, the zener diode between VFET2 and VFET1 would be 3.0V, instead of 4.3V as shown. However, to get a

regulated 3V would require much more current. By using the larger voltage diode with the 100k resistor can provide sufficient, but limited voltage bias, while minimizing the current drain.

It is also important when using an external regulator for the VFETn pins that the regulator have low quiescent voltage and can be disabled when the ISL94208 goes to sleep. The Intersil ISL80136 is an example of a regulator for this application.

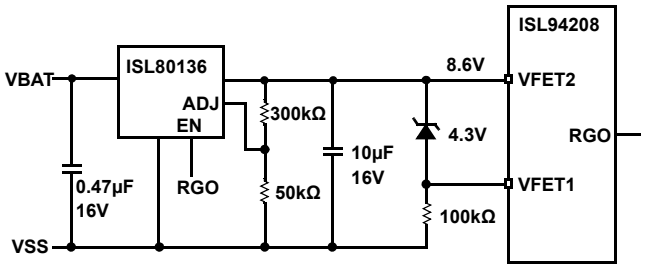


FIGURE 6. ISL94208 EXAMPLE ALTERNATIVE VFET POWER SUPPLY

WKUP Pin Operation

Once the microcontroller puts the ISL94208 to sleep, there are two ways to wake it up again (without power cycling the device). One way uses the WKUP pin in an active LOW mode. The other uses the WKUP pin in an active HIGH mode.

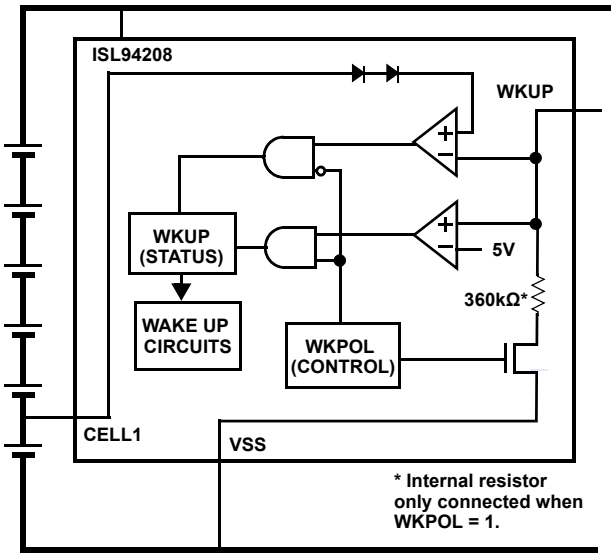


FIGURE 7. INTERNAL WAKE UP CONTROL CIRCUITS

Active LOW WKUP Pin Operation

In an active LOW connection (WKPOL bit = ‘0’ - default), the device can be waken by connecting a load or a charger to the pack (see Figure 8.)

When the pack is asleep, the FETs are off and the WKUP pin is pulled high with a resistor external to the ISL94208. Pulling the pin to the VBACK voltage is recommended. An external supply could be used as long as WKUP is equal to or greater than VCELL1 and less than VFET2.

When the FETs are off, connecting the pack to a load pulls up the gate to the transistor, which turns on and pulls the WKUP pin low. When the WKUP pin voltage goes below the WKUP threshold, the ISL94208 wakes up and turns on the 3.3V voltage regulator.

The capacitor is added to the load connection so there is no quiescent current during normal operation. The capacitor should be large enough to bring WKUP below the threshold for at least 60ms.

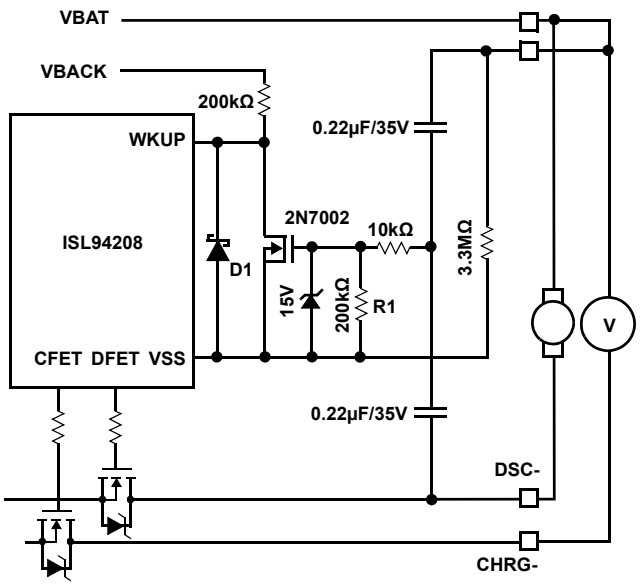


FIGURE 8. WAKE THE ISL94208 WITH LOAD OR CHARGER CONNECTION (WKPOL = LOW)

To wake the pack using a charger, an additional pin and capacitor are added to the circuit of Figure 8. The charger could have connected directly to the WKUP pin to pull it low when the charger connects, however it is shown this way so that there is no drain from VBACK, except during connection of the charger.

In the active low Wake up condition, the pack can also be waken by a microcontroller pulling the WKUP pin low. This assumes that the microcontroller has its own power supply, see Figure 9.

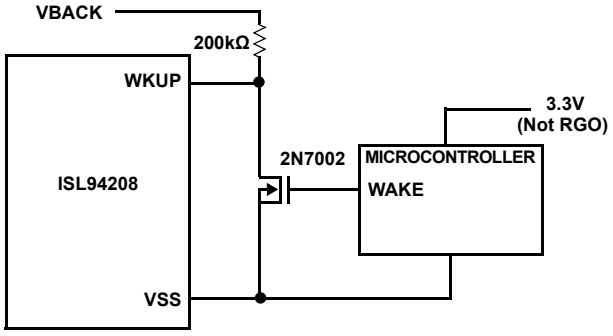


FIGURE 9. WAKE UP THE ISL94208 WITH MICROCONTROLLER. (WKPOL = LOW)

Active HIGH WKUP Pin Operation

In an active HIGH configuration (WKPOL = '1'), the device was designed to wake up when an external switch pulls the pin high. See Figure 10. One of the problems with active high configuration is that if there is a glitch and the contents of the RAM is lost, then the WKPOL returns to 0, so the internal pull down resistor is removed from the circuit. For this reason, even though there is an internal resistor, an external resistor is recommended. To minimize the quiescent current, a capacitor is added to the pull up line.

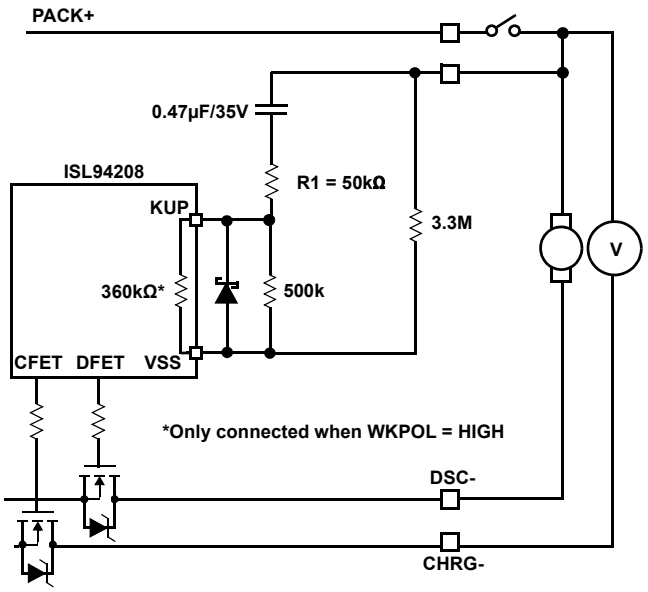


FIGURE 10. WAKE UPTHE ISL94208 WITH EXTERNAL SWITCH (WKPOL = HIGH)

In Figure 10, resistor, R1, combined with a resistor internal to the ISL94208 (and the external parallel resistor,) forms a resistor divider. When a charger or load is switched on, the divider pulls the voltage at the WKUP pin high and wakes up the pack. With no tool or charger connected, the internal resistor pulls WKUP low to prevent the pack from waking up inadvertently.

When the ISL94208 uses the WKUP pin in the active HIGH mode, the external resistor needed to select the proper wake-up threshold is shown in Figure 11 with Equation 1 used for determining the value:

$$R_1 < \left[\frac{CellV(min) \times Numcells}{V_{WKUP1}(max)} - 1\right] \times R_{WKUP}(min) \parallel 500k \quad \text{(EQ. 1)}$$

Assuming a 6-cell pack and a minimum cell voltage of 2.0V, a minimum internal resistance (R_{WKUP}) of 250kΩ (from the data sheet) and a maximum WKUP threshold of 7.5V, Equation 2 for R_1 is:

$$R_1 < \left[\frac{2.0 \times 6}{7.5} - 1\right] \times 168k = 100k\Omega \quad \text{(EQ. 2)}$$

If the WKPOL bit is accidentally reset to 0, then the device does not wake up until the capacitor charges and the WKUP voltage drops back below the V_{WKUP2} (falling edge) threshold.

When WKPOL is 1, an external microcontroller can also wake the pack. as shown in Figure 11.

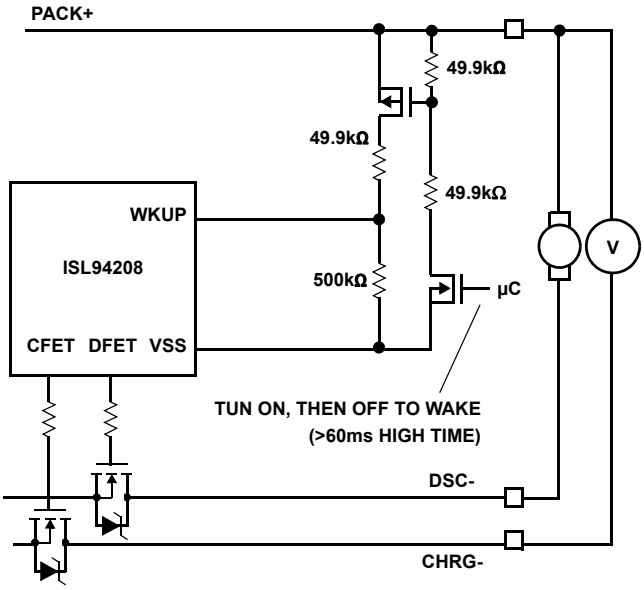


FIGURE 11. WAKE UP THE ISL94208 WITH MICROCONTROLLER (WKPOL = HIGH)

Wake Up Precautions

The circuit designer should consider the conditions listed in the Electrical Characteristics section of the data sheet (see Figure 12) when designing the wake up circuits.

Under normal or sleep conditions, with WKPOL = "0", the WKUP pin should not stay low for long periods. In this condition, the current into the WKUP pin is much higher. This can lead to cell imbalances.

When the WKPOL bit is "1", the VBACK pin draws significant current when the WKUP voltage is near the detection threshold in normal operating mode, and above the threshold in sleep mode. So, the WKUP pin voltage should not remain at voltages above the minimum WKUP threshold for long periods of time. Again, this can lead to cell imbalance.

Another precaution relates to the recommended operating conditions. The data sheet points out that when the WKPOL bit is "1", the WKUP pin can go as high as 27V, but when the WKPOL bit is "0", the maximum voltage on WKUP should be the VFET2 voltage. For this reason, it is probably not a good idea to dynamically switch between the different WKPOL conditions. There is no limit to this, but it may make the external circuits more complicated.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VBACK Input Current (Falling edge wake up; WKPOL = 0) (Normal or Sleep Mode)	$I_{VBACK01}$	WKUP ≤ V_{WKUP2}(max)		7	**12**	µA
	$I_{VBACK02}$	V_{WKUP2}(max) < WKUP < 5V		0.5	**3**	µA
VBACK Input Current (Rising edge wake up; WKPOL = 1) (Normal Mode)	$I_{VBACK11}$	WKUP < V_{WKUP1}(min) or; WKUP > V_{WKUP1}(max)		0.5	**3**	µA
	$I_{VBACK12}$	V_{WKUP1}(min) ≤ WKUP ≤ V_{WKUP1}(max)		120	**300**	µA
(Sleep Mode)	$I_{VBACK13}$	WKUP ≥ V_{WKUP1}(min)		180	**500**	µA
	$I_{VBACK14}$	WKUP < V_{WKUP1}(min)		0.5	**3**	µA

FIGURE 12. VBACK CURRENT AND WAKE UP VOLTAGE RELATIONSHIP (Excerpt from the ISL94208 data sheet)

Power Path Connections

The ISL94208 controls pack operation through one, two, or three power FETs on the negative terminal of the pack. The power FETs can connect in two basic different ways, a single charge/discharge path and separate charge and discharge paths.

Single Charge/Discharge Path

In a single charge/discharge path configuration, the charge and discharge FETs connect back-to-back to provide both discharge and charge protection for the pack (See Figure 13). This is the connection necessary for a “two terminal” pack, in which there is both charge and discharge protection. A variation of this configuration provides the discharge control FET, but no charge control FET.

The DFET output of the ISL94208 actively controls both the turn on and turn off of the discharge FET. When the microcontroller sets the DFET bit in the ISL94208, the ISL94208 outputs a current to the gate of the DFET causing the gate to charge up. When the gate voltage reaches the FET turn on threshold, the FET turns on. The ISL94208 continues to output the turn on current until the voltage reaches the VFET2 voltage. It is clamped at this level.

The CFET output of the ISL94208 actively turns the charge FET on, the same as the DFET output, but the ISL94208 relies on an external resistor to turn off the FET (see Figure 13). This is because the charge FET V_{GS} voltage may go well below the ISL94208 ground voltage when connected to a charger, preventing the ISL94208 from supplying the voltage necessary to turn the FET off. Because of limits to the voltage on the CFET pin, the CFET pin needs a series diode. Also, a zener diode should be used to protect the gate of the charge FET from excessive voltage.

The selection of the charge FET resistor (R1 in Figure 13) is determined by the C_{gs} capacitance of the FET and how fast the charge FET needs to turn off. A resistor value that is too large will not turn the FET off fast enough. Alternatively, a resistor that is too small will clamp the FET gate voltage below the FET turn on threshold. For example, the output current of the ISL94208 CFET pin is 80µA minimum. For a FET with a Vgs of 3V, R_1 needs to be at lease 37.5kΩ or the FET may never turn on.

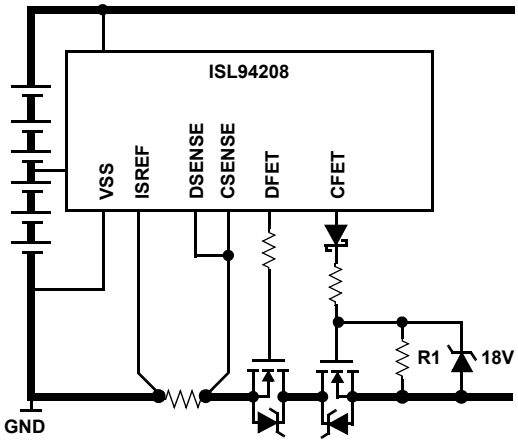


FIGURE 13. BACK TO BACK POWER FETs IN SINGLE CHARGE/DISCHARGE PATH

Figure 13 shows the two FETs being used in a single path. It also shows a sense resistor being used for current monitoring of both discharge and charge current. Because the sense resistor is the same for both charge and discharge, the ratio of the charge overcurrent limits and the charge short circuit limits is primarily determined by the internal threshold settings, however an external resistor divider can provide more flexibility in some situations (see “Current Sense Resistor” on page 12)

Another limitation in the single path configuration is that the charge and discharge FET need to be the same size to handle both the charge and discharge current, even if the charge current is much lower than the discharge current.

An optional single path connection uses only the discharge FET for pack protection. This connection assumes that the external charger protects the cells in the pack from an over charge condition, since the pack electronics will not be able to stop the charge. To do this, the charger communicates with the pack during the charge operation. During this communication, the cell voltages are passed to the charger. These cell voltages become part of the charger over charge limit algorithm.

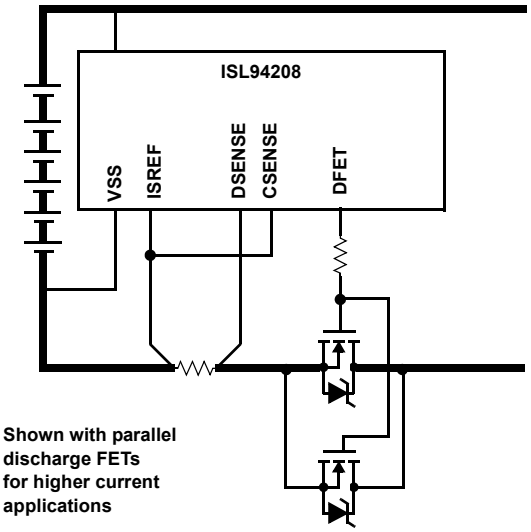


FIGURE 14. DISCHARGE POWER FET ONLY IN SINGLE CHARGE/DISCHARGE PATH

The major advantages of using only a discharge FET are:

- More of the cell voltage is applied directly to the load resulting in less power loss in the pack.
- It is less costly to use the single FET, especially in high current applications where it may be necessary to parallel the power FETs to achieve the necessary current handling capability of the pack.
- This configuration allows the pack to be charged, even if the cell voltages drop too low for the ISL94208 to remain powered.

Separate Charge/Discharge Path

Another method of connecting the power FETs is to provide separate charge and discharge paths. This is shown in Figure 15. In this case, the pack requires only a single discharge FET (Q_1), but requires “back-to-back” charge FETs (Q_2 and Q_3). The charge path needs both FETs because without Q_2, the Q_3 body diode creates a discharge path, even if the discharge FET is off. This can present a safety hazard for the pack.

As shown in Figure 15, the charge current passes through both the charge and discharge sense resistors. The connection is such that if the ISL94208 sees excessive discharge current through the charge path, it will turn off the discharge FETs. With this connection, the charge sense resistance is the sum of the two resistors. However, usually the charge sense resistor is much larger than the discharge sense resistor, so this connection makes little difference.

By designing a separate charge and discharge path, the current sense elements can be different sizes, so the overcurrent threshold limits may be better able to meet the application requirements. Also, since the peak charge current is usually much lower than the peak discharge current, the size (and cost) of the charge FETs can be much less.

The main problem with this connection (in addition to space and cost) is that, small (lower cost) charge FETs may not survive the power dissipation during a short circuit from the charge terminal to the P+ terminal, since the time out is set to protect the higher power discharge FETs.

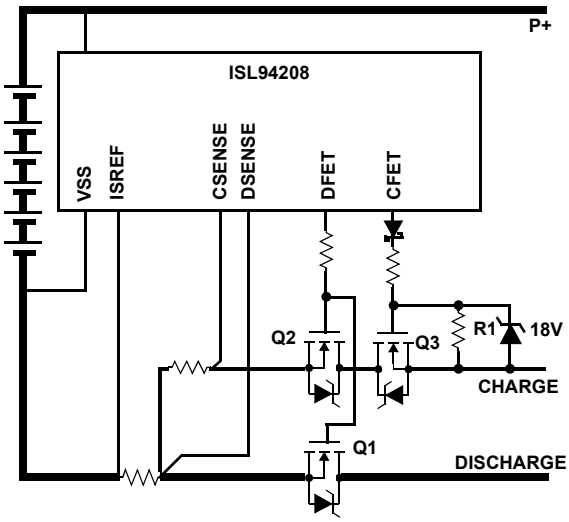


FIGURE 15. POWER FETS IN A SEPARATE CHARGE/DISCHARGE PATH CONNECTION

So care must be taken when using smaller FETs for the charge connection. An alternative is to replace Q_2 with a diode to prevent discharge of the pack by shorting the terminals (see Figure 16.) However, the diode forward current capabilities would need to handle the normal charge current. This requires a relatively large diode that may heat up during charge. Examples of diodes that can be used for D1 include the FYD0504SA from Fairchild or the 1N5404 from various manufacturers.

An alternative connection is shown in Figure 17. In this case, the discharge FET is used in both the separate charge and discharge paths. Here again, there is only a single sense resistor, so this limits the over current setting options.

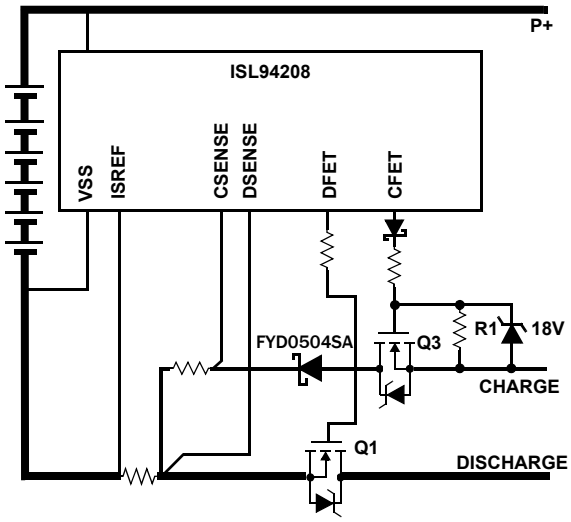


FIGURE 16. POWER FETS IN A SEPARATE CHARGE/DISCHARGE PATH CONNECTION

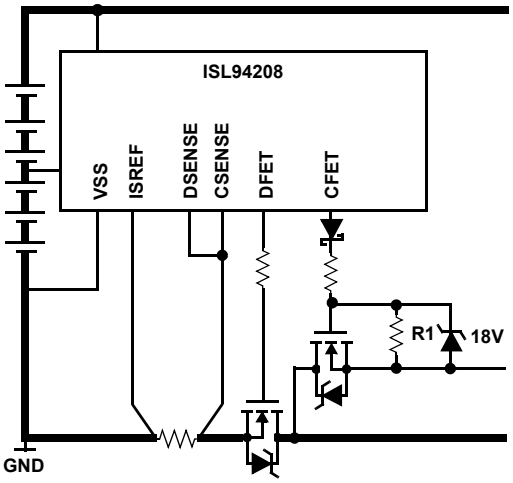


FIGURE 17. BACK TO BACK POWER FETs IN SINGLE CHARGE/DISCHARGE PATH

Special Power Path Connection Guidelines

There are several issues to keep in mind when designing the power control circuit. One of these is the layout of the PCB.

In the recommended connection circuit of Figure 18 below, the ISREF pin connects directly to the sense element and the VSS and the VCELL0 pins connect to the battery negative terminal, using a separate wire for each. There is a wide trace between the current and voltage connections. In actuality, this wide trace will most likely be off board.

The current sense voltage is referenced to the ISREF pin and the cell voltage is referenced to the VCELL0 pin. VSS is connected closer to VCELL0 than ISREF, because the voltage measurements are more sensitive to offsets from ground. The reason for connecting the cells to the board as shown in Figure 18 is because large pack currents can create significant voltage differentials across Wire A. For example, a 40A discharge current creates a voltage drop of 80mV, or more, on a 6 inch, 16 gauge wire segment (see Note 1). If the VSS/VCELL0 pin of the ISL94208 is connected at the terminal of the sense resistor, instead of at the Battery - terminal, the measurement of Cell1 would be off by this 80mV when the pack is discharging 40A of current.

NOTE:

1. Based on resistance for 16 gauge wire of 4.016Ω/1000 feet as listed in the *Handbook of Electronic Tables and Formulas*.

It is recommended that VCELL0 and VSS connect to the battery stack with separate wires. That is because device operating current returning on a combination VSS/VCELL0 wire can affect the measurement by causing a voltage drop on the connecting wire to the negative terminal of Cell1, while there is no commensurate drop on the positive terminal of Cell1.

Since the discharge current is referenced to the ISREF pin (Figure 18), the accuracy is not affected greatly by a high load current. It is necessary, however, to minimize the resistance on the wire as much as possible to prevent the voltage at the ISREF pin from rising too high during a high current event. It is important that the voltage applied at the ISREF pin in a short circuit condition does not exceed the voltage (1.5V – V_{SC}.) For the value of V_{SC}, see data sheet. If this condition is violated, the short circuit detector in the ISL94208 may not work properly.

If it is possible to get a 120A short circuit current, then a 6 inch, 16 gauge wire may not be sufficiently large or the length sufficiently short. A good option is to use a flat braided wire. At smaller gauges these wires provide low resistance to the pack current and offer flexibility for ease of pack assembly.

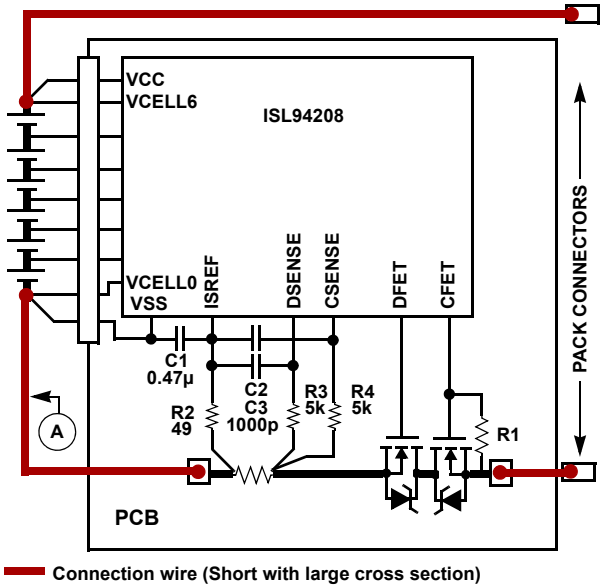


FIGURE 18. PREFERRED BATTERY CONNECTION AND CURRENT SENSE FILTERING

The circuit in Figure 18 also shows filtering for the current sense pins. The ISREF input uses a smaller resistor and a larger overall time constant than the sense input. The sense input resistance of 5kΩ slightly impacts the accuracy of the over current settings, but is not significant. The input current on the discharge sense pin is about 0.25µA, so a 5k input resistor changes the threshold by about 1.25mV or about 1.25%.

High Current/Short Circuit Events

When the ISL94208 turns off the DFET, either as a result of a protection mechanism, or under microcontroller control, the ISL94208 pulls the DFET gate low with a high current (>100mA). This turns off the FET very fast. This fast turn off during a high current discharge can cause a voltage spike on the battery cells due to the inherent inductance of a Li-ion cell. To prevent this voltage spike from damaging the ISL94208, the VCC pin should have an RC filter and a zener diode clamp (see Figure 3.) The diode is used. because the input resistor must necessarily be small to avoid voltage drops on the VCC pin due to device operating current.

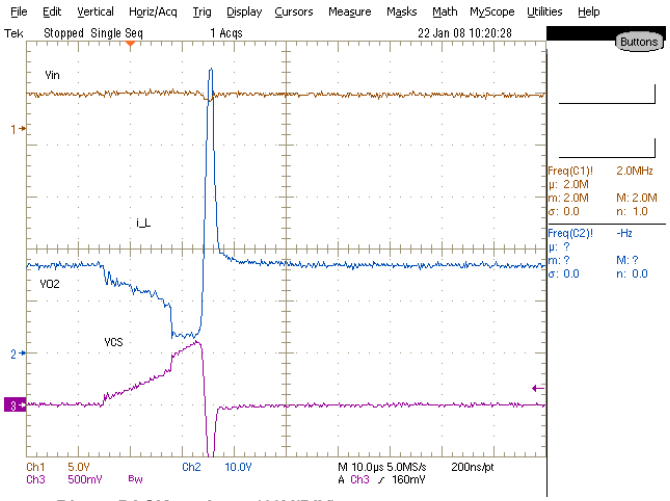
The cell voltage inputs can also be affected by this voltage spike. However, if the input resistors are large enough (1kΩ is recommended), then the resistors limit the current through the device input voltage clamps. If the input resistors are too small, or non existent, then a voltage spike on the cell inputs can

generate enough current to damage the input clamps. Capacitors on the input can be used to absorb some of the energy from this voltage spike, but care should be taken that these input capacitors do not cause hot plug problems. (See "Input Filters" on page 2.)

Another problem that can happen when there is a short circuit of the pack terminals, or a very high load current, is that the internal resistance of the battery cells causes the voltage on the battery pack to drop, sometimes significantly. This varies based on the cells chosen, but the cell voltages during a "dead short" can drop to almost 0V for a brief period of time. If, during the high current event, the cell voltages drop below the POR threshold, or if VBACK and RGO both drop too low, then the ISL94208 detects a power failure and reset the internal registers. This has the effect of turning off the pack, since the CFET and DFET registers are also reset to zero. Because the voltage drops very fast, CFET and DFET turn off with a very short delay, perhaps less than 5µs after the start of the short circuit event.

In order to maintain operation during a very high load condition that can draw the cells to near zero voltage, a large capacitor can be added to the VCC, VBACK, and RGO pins. These capacitors should maintain minimum voltage on the pins for the duration of the low voltage condition. The calculation for the capacitors should include discharge through the input resistors back to the cells and the current into the device pin.

The cell balance inputs might see equal or relatively high voltage spikes. These can also exceed the maximum input specifications and can lead to damage of the ISL94208. So, it is recommended that the cell balance pins have the same input filter time constant as the VCELLn pins.



Blue = PACK+ voltage (10V/DIV)
Purple = 5mΩ current sense voltage (100A/DIV)
Brown = ISL94208 RGO voltage (5V/DIV)

FIGURE 19. EXAMPLE VOLTAGE SPIKE FOLLOWING SHORT CIRCUIT EVENT

Another potential problem when the pack outputs short circuit is one where the voltage on the DFET pin rises above 18V and damages the ISL94208. There are two potential ways to protect this pin. First, through the use of a zener diode (see Figure 20.) This diagram also shows a zener diode on the gate of the transistor to prevent the same short circuit voltage from damaging the DFET.

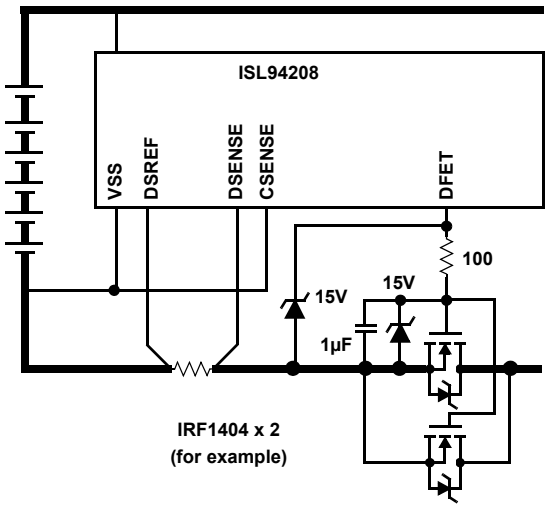


FIGURE 20. DFET PIN PROTECTION DURING SHORT CIRCUIT

A second method of protecting the DFET pin is to use a blocking diode. However, using a blocking diode on the DFET pin means that the ISL94208 is no longer able to turn off the power FET. This requires the addition of a PNP transistor. (See Figure 21.) In this circuit, the DFET pin turns on the DFET directly, but the DFET turns off indirectly through the PNP transistor. The 1k resistor in the base of the PNP transistor limits any current flowing into the DFET pin.

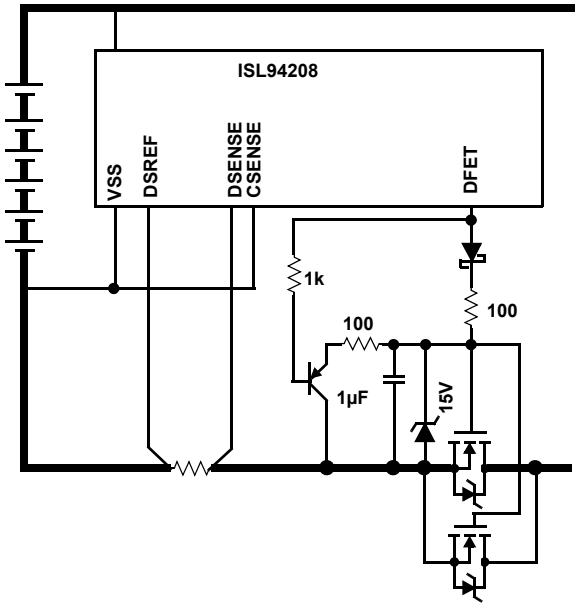


FIGURE 21. ALTERNATE DFET PIN PROTECTION DURING SHORT CIRCUIT

Protection Functions

In the default condition, the ISL94208 automatically responds to discharge overcurrent, discharge short circuit, charge overcurrent, internal over-temperature and external over-temperature conditions. These functions are described in more detail, starting with current protection mechanisms.

Overcurrent Protection Functions

The ISL94208 continually monitors the charge current and discharge current by monitoring the voltage at the CSense and DSense pins (respectively). If either voltage exceeds a selected value for a time exceeding a selected delay, then the device enters an overcurrent or short circuit protection mode. In these modes, the device automatically turns off both power FETs and hence prevents current from flowing through the terminals P+ and P-.

The voltage thresholds and the response times for discharge overcurrent, charge overcurrent, and discharge short circuit conditions are each selected by bits in a control register. In the default condition, the bits are generally set to the safest state. In this condition, the FETs are off, the overcurrent and short circuit settings are at the minimum threshold level and the short circuit setting has the minimum time delay.

See Tables 2 and 3 for threshold and timing options. The power-up condition for all registers is “0”.

TABLE 2. OVERCURRENT VOLTAGE THRESHOLD SETTINGS

REGISTER 5	BIT 6 OCDV1	BIT 5 OCDV0	OVERCURRENT DISCHARGE VOLTAGE THRESHOLD
	0	0	V_{OCD} = 0.10V
	0	1	V_{OCD} = 0.12V
	1	0	V_{OCD} = 0.14V
	1	1	V_{OCD} = 0.16V
REGISTER 5	BIT 3 SCDV1	BIT 2 SCDV0	SHORT CIRCUIT DISCHARGE VOLTAGE THRESHOLD
	0	0	V_{SCD} = 0.20V
	0	1	V_{SCD} = 0.35V
	1	0	V_{SCD} = 0.65V
	1	1	V_{SCD} = 1.20V
REGISTER 6	BIT 6 OCCV1	BIT 5 OCCV0	OVERCURRENT CHARGE VOLTAGE THRESHOLD
	0	0	V_{OCD} = 0.10V
	0	1	V_{OCD} = 0.12V
	1	0	V_{OCD} = 0.14V
	1	1	V_{OCD} = 0.16V

TABLE 3. OVERCURRENT DELAY TIME SETTINGS

REGISTER 5	BIT 1 OCDT1	BIT 0 OCDT0	OVERCURRENT DISCHARGE TIMEOUT
	0	0	t_{OCD} = 160ms (2.5ms if DTDIV = 1)
	0	1	t_{OCD} = 320ms (5ms if DTDIV = 1)
	1	0	t_{OCD} = 640ms (10ms if DTDIV = 1)
	1	1	t_{OCD} = 1280ms (20ms if DTDIV = 1)
REGISTER 6	BIT 1 OCCT1	BIT 0 OCCT0	OVERCURRENT CHARGE TIMEOUT
	0	0	t_{OCC} = 80ms (2.5ms if CTDIV = 1)
	0	1	t_{OCC} = 160ms (5ms if CTDIV = 1)
	1	0	t_{OCC} = 320ms (10ms if CTDIV = 1)
	1	1	t_{OCC} = 640ms (20ms if CTDIV = 1)
REGISTER 6	BIT 4	SCLONG Short circuit long delay	When this bit is set to ‘0’, a short circuit needs to be in effect for 190µs before a shutdown begins. When this bit is set to ‘1’, a short circuit needs to be in effect for 10ms before a shutdown begins.
	BIT 3	CTDIV Divide charge time by 32	When set to “1”, the charge overcurrent delay time is divided by 32. When set to “0”, the charge overcurrent delay time is divided by 1.
	BIT 2	DTDIV Divide discharge time by 64	When set to “1”, the discharge overcurrent delay time is divided by 64. When set to “0”, the discharge overcurrent delay time is divided by 1.

After the ISL94208 detects any overcurrent condition, and both power FETs are turned off, the ISL94208 sets a status flag. A discharge overcurrent condition sets the DOC bit, a charge overcurrent condition sets the COC bit, and a discharge short circuit condition sets the DSC bit. (When the FETs turn off, the DFET and CFET bits also reset to zero.)

Current Monitoring

The ISL94208 monitors the current by comparing the voltage at the CSENSE or DSENSE pins relative to an internal threshold level. An external circuit generates a voltage from the current. Several methods are available for establishing this current limit threshold. These include using a sense resistor, a sense FET, and techniques for translating the FET $r_{DS(ON)}$.

A battery pack with a single charge/discharge path uses the same element to monitor the two different levels of current encountered in an overcurrent condition and a short circuit condition. When designing the current sense circuit, use the setting in Table 4 to pick a setting in which the ratio between the short circuit and overcurrent thresholds most closely matches the desired ratio. (These ratios are shown graphically in Figure 15.) This determines the settings for the ISL94208 discharge thresholds.

TABLE 4. SHORT CIRCUIT TO OVERCURRENT RATIOS

SETTING	SHORT CIRCUIT THRESHOLD	OVERCURRENT THRESHOLD	RATIO
1	1.20V	0.10V	12.0
2	1.20V	0.12V	10.0
3	1.20V	0.14V	8.6
4	1.20V	0.16V	7.5
5	0.65V	0.10V	6.5
6	0.65V	0.12V	5.4
7	0.65V	0.14V	4.6
8	0.65V	0.16V	4.1
9	0.35V	0.10V	3.5
10	0.35V	0.12V	2.9
11	0.35V	0.14V	2.5
12	0.35V	0.16V	2.2
13	0.2V	0.10V	2.0
14	0.2V	0.12V	1.7
15	0.2V	0.14V	1.4
16	0.2V	0.16V	1.3

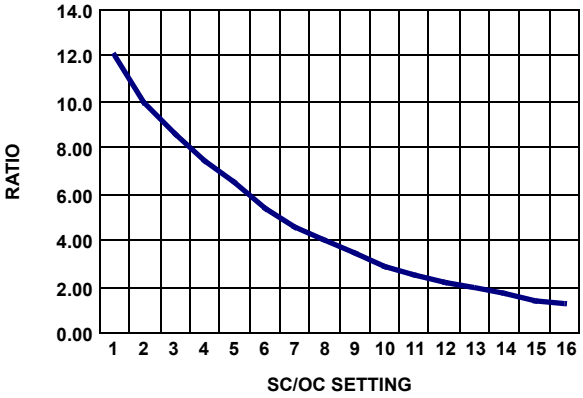


FIGURE 22. SHORT CIRCUIT TO OVERCURRENT RATIO

Current Sense Elements

CURRENT SENSE RESISTOR

Sense resistors (Figure 23) are the easiest and most flexible method of monitoring current in the charge or discharge path (or both). This is a relatively accurate solution, but has some limitations. An application with high current limits will likely require the use of a high power sense resistor or a parallel combination of multiple sense resistors. These can be expensive and will generate heat in the pack. Also, a sense resistor can introduce significant voltage drop and power loss to the load.

In the simplest solution, a sense resistor is used for a relatively low current application (See Example 1 on page 12). In this solution, first select the thresholds and external sense resistor for a pack by using Table 4 to select the closest ratio to the desired short circuit/overcurrent ratio. Use the settings in the table to select the overcurrent and short circuit current thresholds. Next, select a sense resistor that provides the selected overcurrent threshold at the desired current limit. From this, verify the short circuit limit.

Example 1: Designing discharge current limits.

Using the circuit of Figure 13.

Desired Short Circuit Current Level: 15A
Desired Discharge Overcurrent Level: 5A
Ratio (SC/OC): 3.0

Choose Table setting 10: 2.9
Short circuit threshold = 0.35V
Overcurrent threshold = 0.12V

Pick a sense resistor of 0.12V/5A = ~0.025Ω.

Results:
Overcurrent threshold = 4.8A
Short circuit threshold = 14A.

Overcurrent (charge) options: 4A, 4.8A, 5.6A, 6.4A.

With a single charge/discharge path, there are not many options for charge and discharge current limits, since the same resistor is used for both charge and discharge. If the current limits are small enough, the following external circuit can give some flexibility to the pack design (see Figure 23).

In this case, select the sense resistor for the lower of the charge and discharge current limits. The sense resistor provides the voltage for this lower limit. Then, the resistor divider provides the other limits.

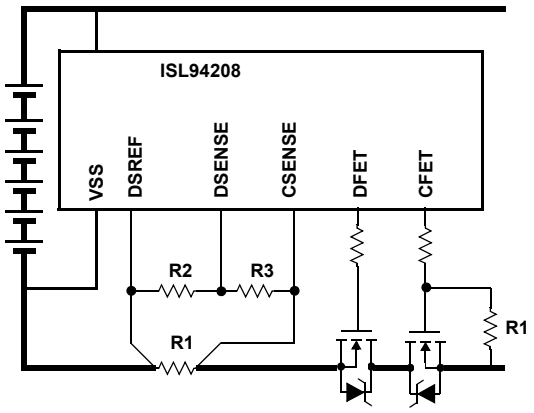


FIGURE 23. USING A RESISTOR DIVIDER TO SELECT CHARGE AND DISCHARGE OVERCURRENT LEVELS

Example 2: Designing discharge and charge current limits using a sense resistor and resistor divider.

Using the circuit of Figure 23.

Desired Short Circuit Current Level:	15A
Desired Overcurrent Level (discharge):	5A
Desired Overcurrent (charge):	2A
Ratio (SC/OC):	3.0
Choose lowest charge O.C. threshold:	0.1V
Choose sense resistor:	0.05Ω

Determine the short circuit to overcurrent ratio:

Choose Table setting 10: 2.9
Short circuit threshold = 0.35V
Overcurrent threshold = 0.12V

Pick a resistor divider of (2A/5A)*(0.12/0.1) = 0.48.
Select the divider resistors:

$$\frac{R_2}{R_2 + R_3} = 0.48 \quad \text{(EQ. 3)}$$

R_2 = 96kΩ
R_3 = 104kΩ

Results:

Overcurrent threshold (charge) =	2A
Overcurrent threshold (discharge)=	5A
Short circuit threshold =	14.6A

While the technique in Example 2 provides a flexible method of addressing the charge and discharge overcurrent settings, it has some limitations. This method requires the use of a larger sense resistor to provide for the use of the voltage divider. In higher current applications this can be a significant drawback. Also, adding the divider resistors can increase the noise of the current measurement circuit.

Consider the next example that does not include the resistor divider, but shows the consequences of using a sense resistor in a high current design.

Example 3: Using a sense resistor in a high current application.

Desired Short Circuit Current Level:	120A
Desired Overcurrent Level:	20A
Ratio (SC/OC):	6.0
Choose Table setting 10:	6.5

Short circuit threshold = 0.65V
Overcurrent threshold = 0.1V

Pick a sense resistor of 0.1V/20A = ~0.005Ohm.

Results:
Overcurrent threshold = 20A
Short circuit threshold = 130A.

Power dissipation in resistor at 20A: 2W
(could be continuous)
Select 5W resistor to minimize heating.
Power dissipation at 120A: 72W
(until SC shutdown)

Overriding Automatic Overcurrent Response

An alternative method of providing the protection function, if desired by the designer, is to turn off the individual automatic overcurrent responses in the ISL94208. See Table 5 for control bits that turn off the automatic control. In this case, the ISL94208 device still monitors the conditions and sets the status bits, but it takes no action in overcurrent or short circuit conditions. Safety of the pack depends, instead, on the microcontroller to send commands to the ISL94208 to turn off the FETs.

TABLE 5. AUTOMATIC CURRENT RESPONSE OVERRIDE SETTINGS

REGISTER 5	BIT 7	DENOCD Turn off automatic OC discharge control	When set to '0', a discharge overcurrent condition automatically turns off the FETs. When set to '1', a discharge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the DOC bit, which also turns on the TEMP3V output.
REGISTER 5	BIT 4	DENSCD Turn off automatic SC discharge control	When set to '0', a discharge short circuit condition turns off the FETs. When set to '1', a discharge short circuit condition will not automatically turn off the FETs. In either case, the condition sets the SCD bit, which also turns on the TEMP3V output.
REGISTER 6	BIT 7	DENOCC Turn off automatic OC charge control	When set to '0', a charge overcurrent condition automatically turns off the FETs. When set to '1', a charge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the COC bit, which also turns on the TEMP3V output.

To facilitate a microcontroller response to an overcurrent condition, especially if the microcontroller is in a low power state, the charge overcurrent flag (COC), discharge overcurrent flag (DOC), or short circuit flag (DSC) being set causes the ISL94208 TEMP3V output to turn on and pull high (see Figure 25 on page 16). This output can be used as an external interrupt by the microcontroller to wake-up quickly to handle the overcurrent condition.

When an overcurrent or short circuit condition occurs and the delay time elapsed, the DSC, DOC, or COC bits are set in the Status register (addr: 01H).

One way to use these status bits is to design the system such that the microcontroller is in a sleep state to conserve power. It uses both a timer and the TEMP3V input as interrupt sources. The microcontroller periodically wakes up to monitor the cells and goes back to sleep. In an “emergency” overcurrent condition, the microcontroller wakes up in response to the TEMP3V interrupt and turns off the FETs.

In practice, when any of the three overcurrent status bits are set, the TEMP3V output turns on and does two things:

1. This turns on the ISL94208 external over-temperature monitor circuit. (There is no harm in turning this on too often, except that the circuit consumes about 400µA of current until TEMP3V turns off).
2. If the microcontroller is in a sleep mode, TEMP3V wakes up the microcontroller by applying a voltage to the interrupt. When the microcontroller services the interrupt, it reads the status register to determine if there was an overcurrent or short circuit condition. Reading the status register resets the status bits, which turns off the TEMP3V output.

If the microcontroller is not in the sleep mode the microcontroller can disable the TEMP3V interrupt, so that a TEMP3V input does not disrupt other code, or it can leave the interrupt on to provide the microcontroller a hardware response to an overcurrent condition. If the interrupt is left on, then reading the external temperature with the A03:A00 bits also causes an interrupt to the microcontroller. But a simple scan of the status register indicates whether this was an overcurrent condition, or a normal temperature scan.

Load Monitoring

Once the power FETs turn off as a result of an overcurrent condition, they are not automatically turned back on by the ISL94208. They are turned on again by the external microcontroller. The micro can turn on the FETs right away, but if the load or short circuit is still present, there will be a big current surge through the FETs. If this turn-off and turn-on oscillation is not controlled, then the FETs can heat and possibly fail. So, before the microcontroller turns on the power FETs after an overcurrent condition, it is best to check to see if the load has been removed before turning the FETs on again.

DISCHARGE LOAD MONITORING

For pack discharge conditions, the ISL94208 provides a mechanism for detecting the removal of the load from the pack following an overcurrent or short circuit condition. This is called the load monitor and uses the VMON pin on the ISL94208.

The load monitor function is normally inactive to minimize current consumption. To use it, the microcontroller must activate the circuit. It works by internally connecting the VMON pin to VSS through a resistor. This internal resistor and the external load form a voltage divider with the VMON pin reflecting the divided voltage. The VMON pin is compared to an internal reference. If VMON is above the reference, then the pack load is still present. If the voltage at VMON is below the threshold, then the load has been released enough to allow the power FETs to be turned on again. The circuit operates shown as in Figure 24.

In operation, when an overcurrent or short circuit event happens, the discharge and charge FETs turn off. At this time, the R_L resistance is small and the load monitor is off. As such, the voltage at VMON rises to nearly the pack voltage.

Once the power FETs turn off, the microcontroller activates the load monitor by setting the LDMONEN bit. This turns on a FET that activates the current sink in the load monitor circuit. While still in the overload condition, the combination of the load resistor, an external adjustment resistor (R_1), and the internal resistor form a voltage divider. R_1 is chosen so that when the load is released to a sufficient level, the LDFAIL condition resets. For the ISL94208, the value of R_1 can be zero.

Diode D_4 is optional and prevents the voltage at the VMON pin from going higher than the maximum rated voltage if there is a voltage spike on the pack pine and it prevents the voltage from going negative when the charger is connected. The pin is rated at V_{SS} - 22V, so the device should not be affected by the negative voltage, but if there is concern about the pin, the diode will protect VMON, while not affecting the performance of the circuit.

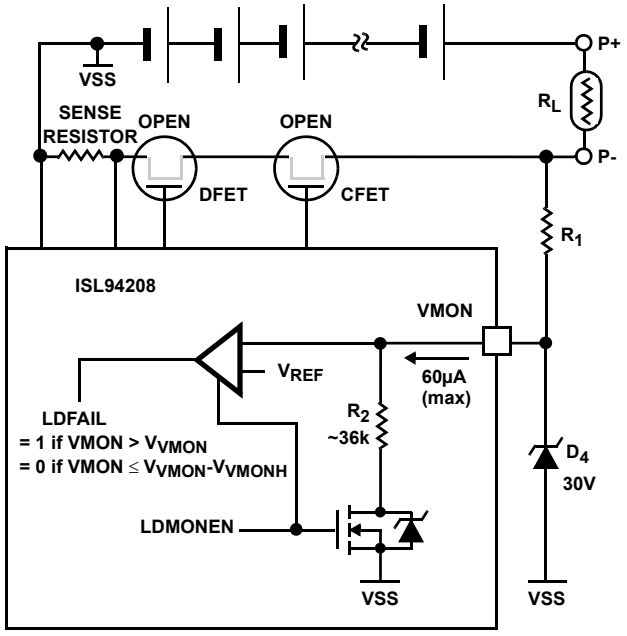


FIGURE 24. LOAD MONITOR CIRCUIT

Load Monitor Example:

Removing an overcurrent or short circuit condition results in the value of R_L increasing. Use Equation 4 to determine at what resistance the load monitor will detect the release of the load. This allows the calculation of the value for R_1.

$$R_L + R_1 \geq \frac{(CellV \times Numcells) - V_{VMON}(max)}{I_{VMON}(max)} \quad \text{(EQ. 4)}$$

For a 6-cell pack, the minimum combined resistance at a pack voltage of 25.2V (ISL94208: 6-cells) is:

$$R_L + R_1 \geq \frac{25.2 - 1.8V}{60\mu A} = 390k\Omega \quad \text{(EQ. 5)}$$

At a depleted pack voltage of 2.5V per cell, P+ is 15V and the $R_L + R_1$ resistance is 220kΩ.

At the opposite extreme, for a fully charged pack (based on ISL94208 parameter variations):

$$R_L + R_1 \geq \frac{(CellV \times Numcells) - V_{VMON}(min)}{I_{VMON}(min)} \quad \text{(EQ. 6)}$$

$$R_L + R_1 = \frac{25.2 - 1.1V}{20\mu A} = 1.205M\Omega \quad \text{(EQ. 7)}$$

The R_L+R_1 for a fully depleted pack 695kΩ. These values are summarized in Table Table 6.

TABLE 6. R_L+R_1 OVERCURRENT RECOVERY RESISTANCE

RL + R1	FULLY CHARGED PACK	FULLY DEPLETED PACK
Max VMON current Max VMON threshold	390kΩ	220kΩ
Min VMON current Min VMON threshold	1.205MΩ	695kΩ

The value of R_1 is set to be anything from 0Ω to 262kΩ. Using 262kΩ is not desired, because in a fully depleted system, under worst case conditions, the RL + R1 resistance could always indicate that the over current condition is released, even if it is not.

Using an R1 resistance value of 0Ω is also not desired, because high voltage transitions (>36V) on the VMON pin, due to any voltage spikes, would have no input current limiting into the pin ESD structure. A minimum of 1kΩ is recommended for R1.

CHARGE LOAD MONITORING

The ISL94208 load monitor circuit does not provide detection of charger removal after a charge overcurrent condition, because it is likely that the voltage on the charger will be higher than the pack voltage and the VMON pin would be negative.

In the event that the pack FETs turn off due to an overcurrent condition during charge, the microcontroller will need to use a timing based procedure for turning the FETs on again. The recommended procedure for responding to a charge overcurrent is to wait for a period of time, then turn the FETs on again. This delay time is dependent on the choice of FETs and its power handling capabilities. The time should be set long enough for the FET to cool off.

After the FET turns back on, if another charge overcurrent happens within a fixed time period, then the microcontroller might decide to wait much longer before turning the FETs on or it might keep the FETs off (effectively disabling the pack). Repetitive overcurrent conditions during charge could indicate a pack failure, charger failure, or the use of the wrong pack/charger combination. The specific algorithm requirements are up to the pack/system designer.

Over-Temperature Safety Functions

EXTERNAL TEMPERATURE MONITORING

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL94208 TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, the ISL94208 continuously turns on TEMP3V output (and the external temperature monitor) for 4ms every 512ms. In this way, the external temperature is monitored even if the microcontroller is asleep. If the ATMPOFF bit is set, this automatic temperature scan is turned off.

The TEMP3V pin turns on when the microcontroller sets the A03:A00 bits to select that the external temperature voltage be placed A0. As long as the A03:A00 bits point to the external temperature the TEMP3V output remains on.

The microcontroller can over-ride both the automatic temperature scan or the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns the TEMP3V output on all the time to keep the temperature control voltage on indefinitely. This will consume a significant amount of current, so it is likely this feature would be used for special or test purposes.

When the TEMP3V output is on, the external temperature voltage is compared with an internal voltage divider that is set to TEMP3V/13. When the voltage is below this threshold for more than 1ms, the external temperature fail condition exists.

To set the external over-temperature limit, determine the resistance of the desired thermistor at the temperature limit. Then, select a fixed resistor that is 12x that value.

Example 4: Selecting the resistor/thermistor for external over-temperature limit.

Selected Thermistor: MuRata XH series
Desired Over-Temperature Limit: +55°C
Thermistor resistance at limit: 3.54kΩ

Calculate R_X value (see Figure 25):
3.54kΩ*12 = 42.48kΩ
Pick an R_X resistor: 42.2kΩ

Results:
Calculated temperature threshold: 42.2kΩ/12 = 3.517V
Temperature limit (MuRata table look up): +55.17°C

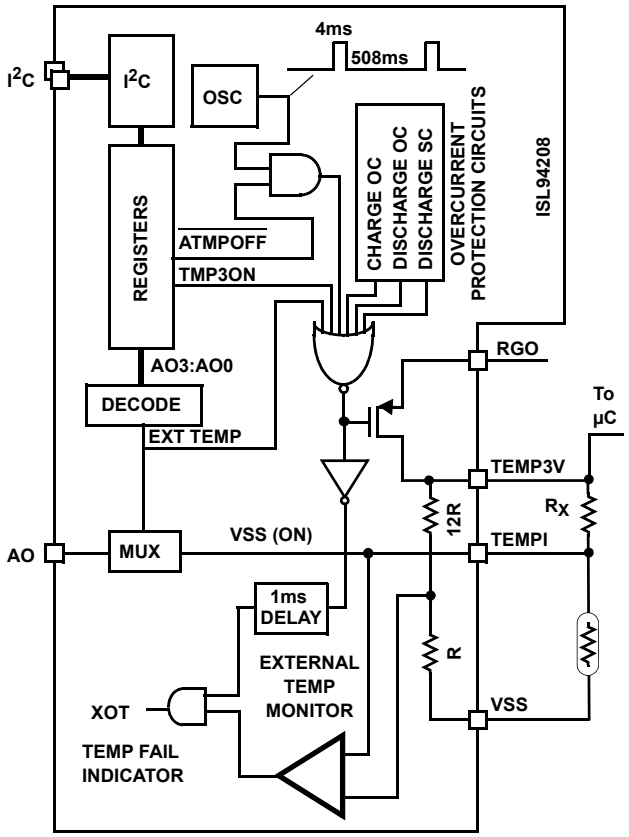


FIGURE 25. EXTERNAL TEMPERATURE MONITORING AND CONTROL

PROTECTION

When the ISL94208 detects an internal or external over-temperature condition, the FETs are turned off, the cell balancing function is disabled, and the IOT bit or XOT bit (respectively) is set.

While in an over-temperature condition, the ISL94208 prevents cell balancing and the power FETs are held off. This continues until the temperature drops back below the temperature recovery threshold. During a temperature shutdown, the microcontroller can monitor the internal temperature through the analog output pin (AO), but any writes to the CFET bit, DFET bit, or cell balancing bits are ignored.

The automatic response for the ISL94208 was chosen to prevent damage to the IC, the cells, and the pack. If the internal temperature reaches the internal temperature limit, it is most likely due to heating from cell balancing, perhaps as a result of a faulty microcontroller or runaway code. Keeping the cell balance resistors on when the ISL94208 internal temperature is above the threshold temperature is not advised.

If the ISL94208 detects the external temperature reaching its limit, it is possible that the cells are over heating due to a fast charge or discharge. The external temperature protection circuit turns the power FETs off to prevent further heating, which can lead to thermal runaway in some cells. Turning off the cell balance also limits the discharge from the cells to minimize heating.

If this automatic response is not desired, the microcontroller can prevent an automatic shutdown of the power FETs and cell balancing operation after either an internal or external over-temperature detect by setting the DISITSD bit to “1” (internal temperature) or the DISXTSD bit to “1” (external temperature). In either of these cases, the IOT and XOT bits continue to be set, to indicate an over-temperature condition, but it is up to the microcontroller to detect the condition and respond.

Analog Multiplexer Selection

The ISL94208 individually provides battery cell voltages and temperatures on the AO pin. Using the I²C interface, the microcontroller selects the voltage to be monitored, then uses its internal A/D converter to monitor the AO voltage (see Figure 26).

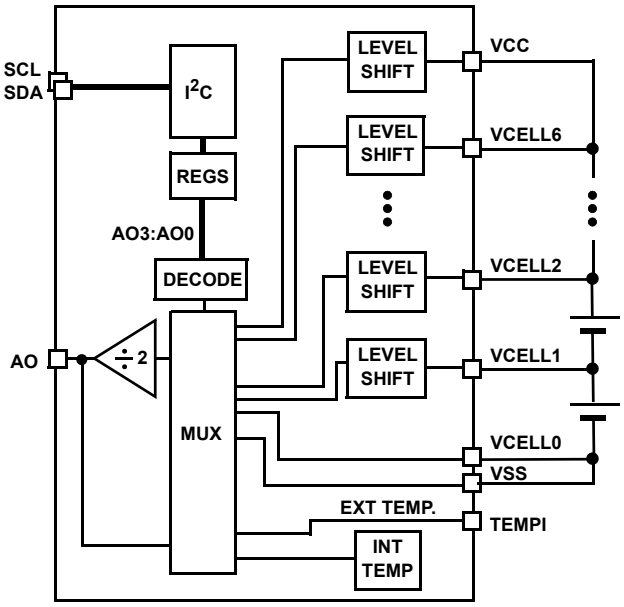


FIGURE 26. ANALOG OUTPUT MONITORING DIAGRAM

The output of the AO pin is sensitive to noise in the system, but the ability to filter the output is minimal. First, a resistor in series with the AO pin and the A/D input can result in a voltage drop, if the input impedance of the A/D converter is low. Second, the ISL94208 AO amplifier does not handle large capacitance loads very well.

There are two ways to approach this. First, the use of a ΣΔ A/D converter provides some inherent filtering, so the noise showing up on AO is inconsequential. If using a successive approximation A/D, then an RC filter may be required. For this filter, the recommendation is a series resistor of 500Ω and a filter capacitor of 1000pF.

The ISL94208 evaluation board uses a 500Ω resistor in series with the Freescale microcontroller A/D input, which results in a voltage drop of 0.5mV at an AO voltage of 1.75V. The RC combination reduces the noise significantly and has little ringing. However, the AO output does have a longer settling period after a large jump in the AO voltage, so a delay of 10µs is recommended between changing the AO output and sampling with the A/D converter. This is usually shorter than the time required to terminate the I²C communication that selects the AO source, so usually no extra code or delay timing is required.

Operating Performance (RGO)

Following are some characterization data gathered over 30 units. This shows the regulation accuracy from no load to a load of 500µA on the RGC pin (this would be 50mA on RGO when using a 100 gain NPN transistor). Typically, the load will be much less than the maximum load, so the variation of RGO will be much less. But, if the microcontroller A/D converter accuracy is dependent on the RGO voltage, then a calibration step is likely needed to trim the accuracy of the A/D for cell voltage measurements. Generally, this calibration can be done once at room temperature, because the variation over temperature is low. However, for measurements more accurate than ±25mV at a cell voltage of 4.2V, a voltage reference for the microcontroller A/D converter is recommended.

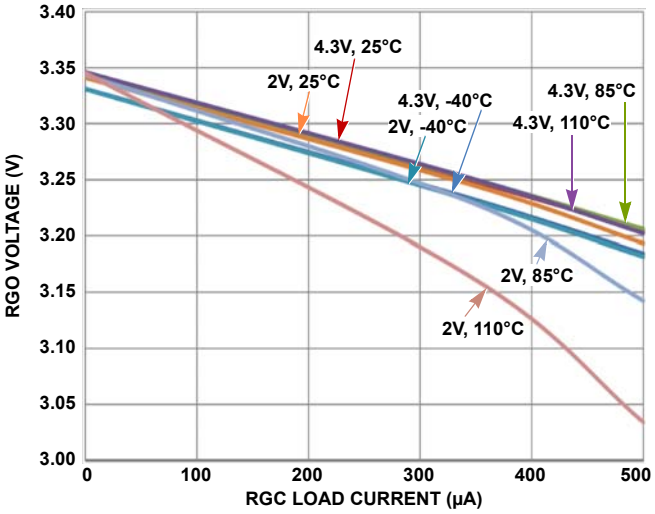


FIGURE 27. RGO VOLTAGE OVER LOAD, TEMPERATURE, AND CELL VOLTAGE (4.3V AND 2V)

Voltage Monitoring

Since the voltage on each of the Li-ion Cells are normally higher than the regulated supply voltage, the ISL94208 both level shifts and divides the voltage from the cells. To get into the voltage range required by the external A/D converter, the voltage level shifter divides the cell voltage by 2. Therefore, a Li-ion cell with a voltage of 4.2V is reported via the AO pin to be 2.1V.

The variation in the cell voltage from cell to cell is typically less than the variation from device to device. The variation of any cell voltage over the voltage range of the cells is less than the variation of the cell to cell voltage, and the variation of the output of any one cell over-temperature is even less. As such, the addition of a calibration step when testing the PCB can significantly improve the performance of the design. Below are characterization data showing the accuracy of the ISL94208. The following data was taken over 30 units.

Figures 28 and 29 show absolute error with the results of each cell compared to the input voltage. The data shows the minimum and maximum extremes of error for each cell. These figures show the device-to-device variation.

$$\text{Error} = \text{AppliedCellVoltage} - (\text{AO} \times 2) \quad \text{(EQ. 8)}$$

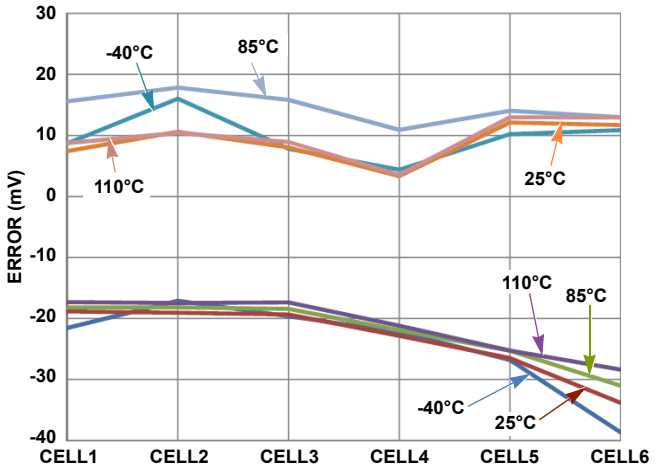


FIGURE 28. MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 2.3V

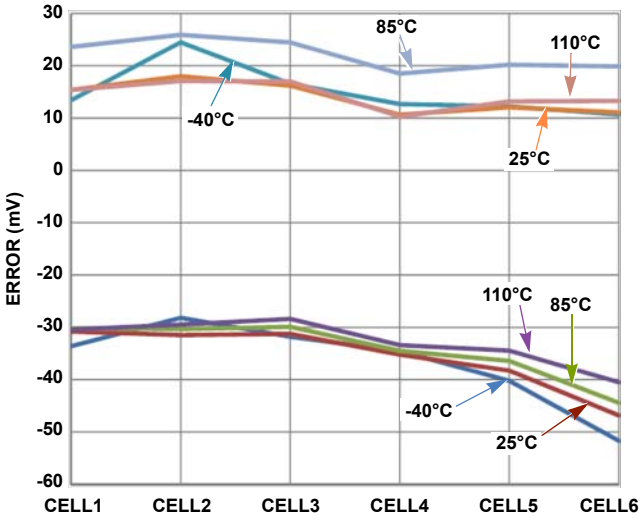


FIGURE 29. MIN/MAX ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 4.3V

For Figures 30 and 31, the error for the cells on each device was compared with the error on cell3 of that same device according to Equation 9:

$$\text{Error} = \text{ErrorCell}_N - \text{ErrorCell}_3 \quad \text{(EQ. 9)}$$

Then, the graph shows the minimum and maximum errors over the 30 units. This gives the minimum and maximum variation of error for any one device.

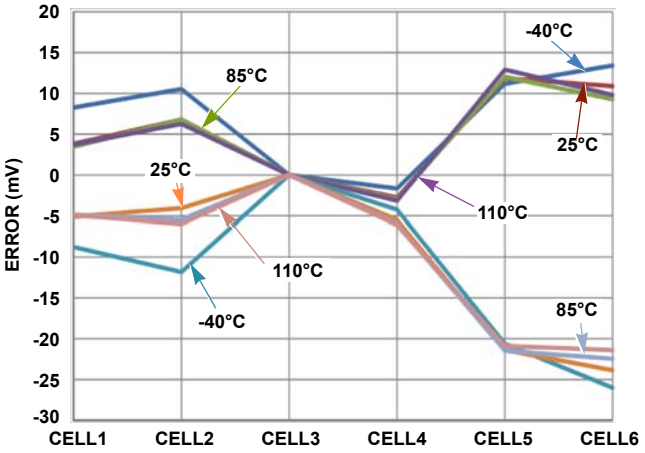


FIGURE 30. MINIMUM AND MAXIMUM ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 2.3V, RELATIVE TO 2.3V

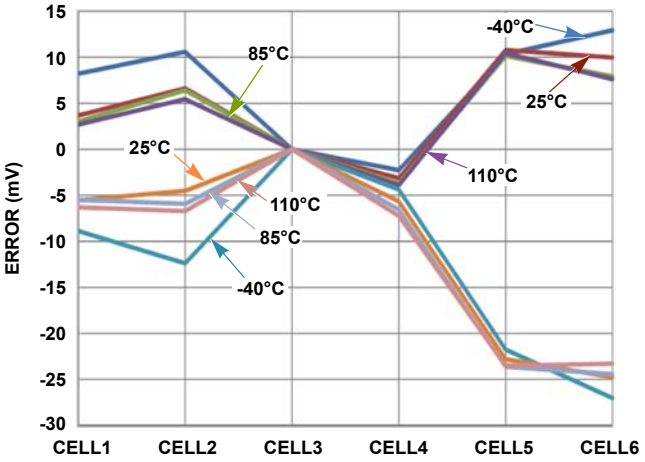


FIGURE 31. MINIMUM AND MAXIMUM ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 4.3V RELATIVE TO 4.3V

For Figure 32, it is assumed that the error at room temperature and 4.3V per cell for each device and for each cell is zero. Then the error at 2.3V is compared with the error at 4.3V for the same device and same cell inputs on that device. The comparison uses the Equation 10:

$$Error = ErrorCell_N(2.3V) - ErrorCell_N(4.3V) \quad \text{(EQ. 10)}$$

The chart in Figure 32 shows all of the errors over the 30 units and all cell inputs.

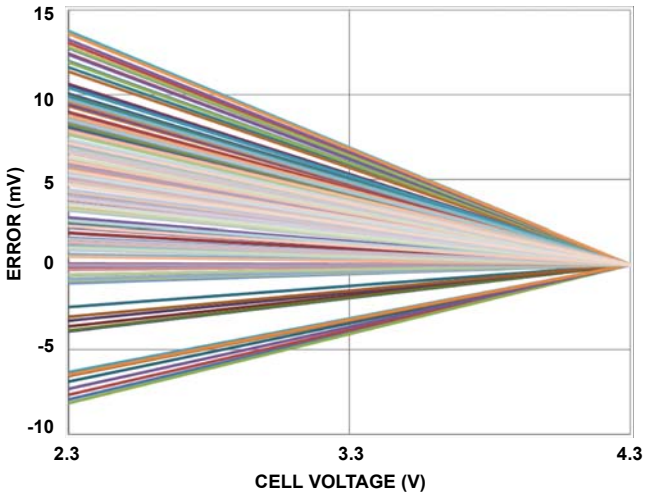


FIGURE 32. ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES FROM 2.3V TO 4.3 (RELATIVE TO 4.3V)

For Figures 33 and 34, the error for the cells on each device over temperature are compared with the error on same device at room temperature, according to the Equation 11:

$$Error = ErrorCell_N(OverTemp) - ErrorCell_N(Room) \quad \text{(EQ. 11)}$$

Then, the graph shows the minimum and maximum errors over the 30 units at two different cell voltages.

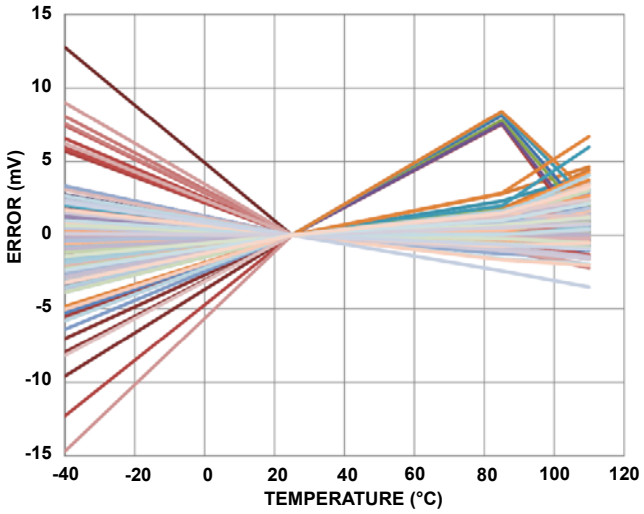


FIGURE 33. ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 2.3V RELATIVE TO 25°C

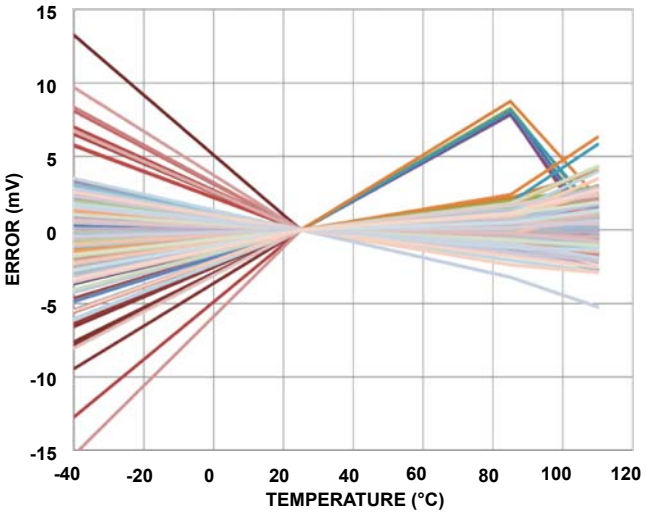


FIGURE 34. ANALOG OUTPUT ERROR FOR 30 UNITS AT CELL VOLTAGES OF 4.3V RELATIVE TO 25°C

Because the accuracy of the ISL94208 is better when looking at each device (rather than assuming all devices are the same) and because the variation of the voltage measurement is less over voltage and temperature, the performance of the ISL94208 can be improved by performing a calibration at room temperature after the board is assembled.

A calibration procedure might consist of the following steps:

1. Power the board and program the microcontroller with standard pack code, using the microcontroller internal Flash and a download interface. Next, power down the board, so on re-start the pack code is operational.
2. Power-up again with a known voltage of 3.300V on every cell input (room temperature is OK). This powers the board and starts the microcontroller. The downloaded microcontroller code runs normally, and assumes that there are no errors in the cell voltage readings. However, the code includes a calibration mode that is activated through a debugger or a dedicated pin.
3. Use the debugger or pin to start the calibration mode. Inside the microcontroller, the code successively selects each cell input and compares the cell voltage reading with the expected 3.30V input. Any differences are temporarily stored in separate locations in RAM. It is more important to calibrate at 3.3V than other values, because this is in the flat part of the discharge curve and accuracy is more critical in this area.
4. After all cell voltages are read, the code writes the offset values to Flash and uses these calibration values in future scans of the cells.

An alternative technique does not require accurate voltage sources, but instead uses an accurate measurement of the inputs. In this case, the A/D conversion results are compared with the meter readings of each input and the delta is saved to Flash.

The process of powering up the board, programming it, and calibrating the inputs should take less than 15s. Most of this time is taken up by the initial download of the microcontroller code and this process can be completed before connection of the board to the battery cells.

Below is an example of the calibration accuracy over cell voltages based on the ISL94208EVAL2Z board. The board was calibrated one time at room temperature, with cell voltages of about 3.3V. The board used 1kΩ series input resistors on the VCELLn pins. In this case, the microcontroller has a 10-bit ADC. A 10-bit ADC has a minimum resolution of about 3.2mV, so this limits the accuracy of the initial calibration and subsequent measurements. Better calibration could be done using a higher resolution ADC monitoring the AO pin on the board. Figure 35 shows the absolute error measured for each cell. Figure 36 shows the error over voltage after trimming at 3.6V.

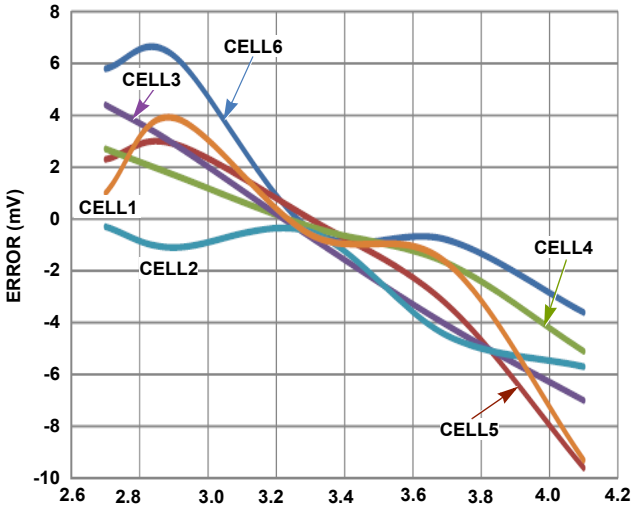


FIGURE 35. CELL VOLTAGE ACCURACY AFTER CALIBRATION AT 3.3V (ROOM TEMP)

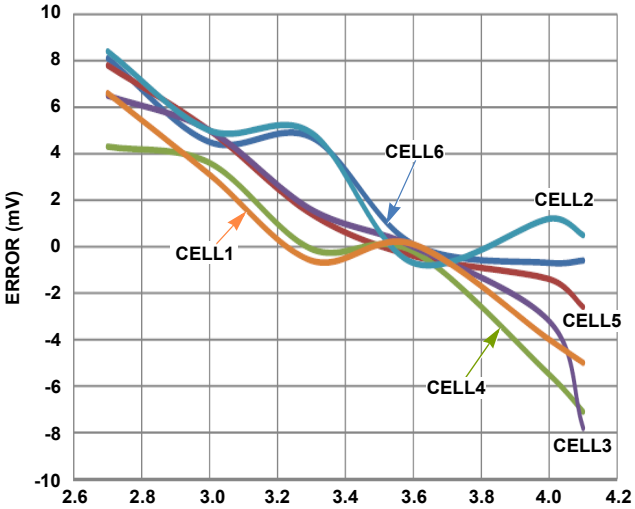


FIGURE 36. CELL VOLTAGE ACCURACY AFTER CALIBRATION AT 3.6V (ROOM TEMP)

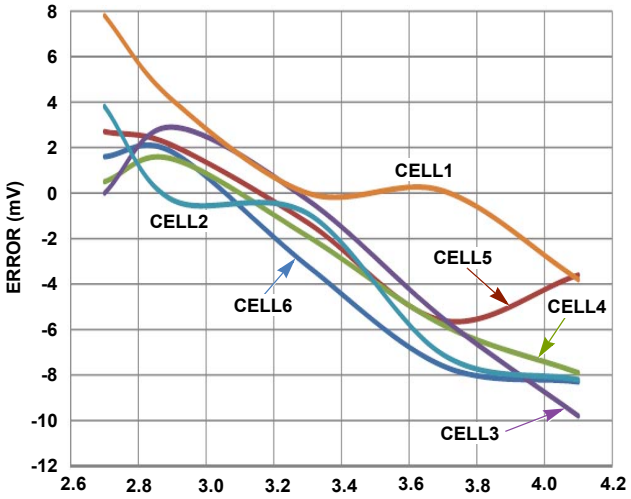


FIGURE 37. CELL VOLTAGE ACCURACY WITH 20Ω SERIES RESISTORS AFTER CALIBRATION AT 3.3V, ROOM TEMP, AND WITH 1k SERIES RESISTORS

By trimming at room temperature and a specific voltage, the battery management circuit can provide better results than the absolute accuracy, un-calibrated numbers shown above. For the 30 units tested, the results were analyzed assuming a trim at 4.3V and room temperature. From this data, the worst case high and low errors over both temperature (-40°C to +85°C) and voltage (2.3V to 4.3V) were recorded. These errors were binned to provide a histogram. These data are shown in Figure 38.

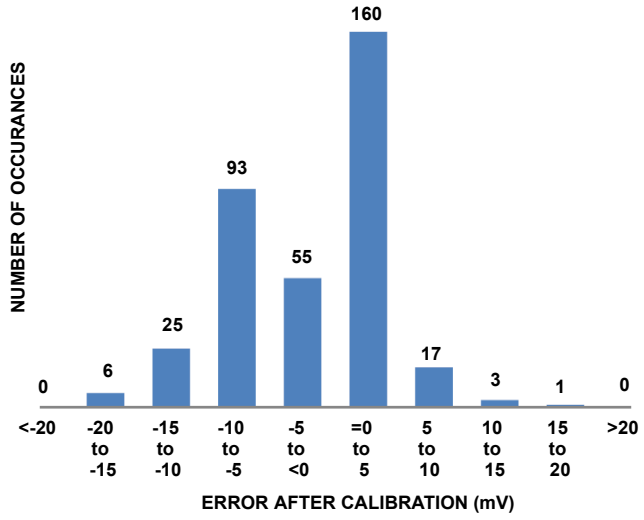


FIGURE 38. MAX/MIN ERROR OVER VOLTAGE AND TEMPERATURE FOR 30 UNITS, ALL CELLS (AFTER CALIBRATION)

Temperature Monitoring

The voltage representing the external temperature applied at the TEMPI terminal is directed to the AO terminal through a MUX, as selected by the AO control bits (see Figures 25 and 26.) The external temperature voltage is not divided by 2 as are the cell voltages. Instead it is a direct reflection of the external temperature voltage divider. The microcontroller takes this monitored voltage and typically converts it to a temperature using a table. To get resolution of less than +5°C, there typically needs to be some interpolation between table set points. See some sample code in Figure 39. In this code, the table values are the voltage, in mV for each 5°C step applied to the input (based on an external 46.4k resistor and the specified Murata thermistor.)

A similar hardware operation occurs when monitoring the internal temperature through the AO output, except there is no external “calibration” of the voltage associated with the internal temperature. For internal temperature monitoring, the voltage at the output is linear with respect to temperature and has a slope and offset. (See Operating Specifications for information about the output voltage at +25°C and the output slope relative to temperature.) Based on the data sheet, an equation that translates internal temperature in volts to internal temperature in °C is:

$$\mathrm{IntTemp}(°C) = \frac{AO_{\mathrm{IntTemp}} - 1.31}{-0.0035} + 25 \qquad \text{(EQ.12)}$$

where $AO_{IntTemp}$ is measured in volts.

Cell Balancing

Overview

A typical ISL94208 Li-ion battery pack consists of four to six cells in series, with one or more cells in parallel. This combination gives both the voltage and power necessary for power tools, e-bikes, electric wheel chairs, portable medical equipment, and battery powered industrial applications. While the series/parallel combination of Li-ion cells is common, the configuration is not as efficient as it could be, because any capacity mismatch between series-connected cells reduces the overall pack capacity. This mismatch is greater as the number of series cells and the load current increase. Cell balancing techniques increase the capacity, and the operating time, of Li-ion battery packs.

There are two kinds of mismatch in the pack, State-of-Charge (SOC) and capacity/energy (C/E) (Note 2) mismatch, with SOC mismatch being more common. Each problem limits the pack capacity (mAh) to the capacity of the weakest cell. It is important to recognize that the cell mismatch results more from limitations in process control and inspection than from variations inherent in the Lithium Ion chemistry.

NOTE:

2. In SOC mismatch, the cells all have the same inherent capacity, but through charge and discharge inefficiencies, they have arrived at a condition where the state of charge are different cell to cell. In C/E mismatch, the cells begin with different inherent capacities. In this type of mismatch, an imbalance between cells is inherent in the pack, even if there are no charge/discharge inefficiencies. Because Li-ion manufacturing is improving, the C/E mismatch is less common.

The use of cell balancing can improve the performance of series connected Li-ion Cells by addressing both State-of-Charge and Capacity/Energy issues. SOC mismatch can be remedied by balancing the cell during an initial conditioning period and subsequently only during the charge phase. C/E mismatch remedies are more difficult to implement and harder to measure and require balancing during both charge and discharge periods.

```
/*************************************************************************************************
This function converts voltage from the AO output to external temperature. It uses a table lookup
based on the muRata NCP03XH103J05RL thermistor */

short calculate_externaltemp(short voltage)
{
unsigned short Rtable[22]={
1963, 1768, 1577, 1393, 1219, 1061, 918, 793, 682, 585, 501, 429, 368, 316, 271, 233, 201, 174, 151,
131, 114, 100
};
 char i,j;
 short temperature;
 short temp1, temp2;

 for(i=0;i<22;i++){
    if(scan_control.ISL94208Temp[0] > Rtable[i])
      break;
 }
 temperature = (-20+i*5);

 /* use the following formula to interpolate values inside a 5degree grid
 temperature = (-20+i*5) + ((scan_control.ISL94208Temp[0]-Rtable[i]) * -5)/(Rtable[i-1]-Rtable[i]);
 */
 temp1 = scan_control.ISL94208Temp[0]-Rtable[i];
 temp1 = 5*temp1;
 temp2 = Rtable[i-1]-Rtable[i];
 for(j=0;j<5;j++){
    if(temp1<(j+1)*temp2)
      break;
 }
 temperature += (4-j);

 return temperature;
}
```

FIGURE 39. SAMPLE CODE FOR CONVERTING EXTERNAL TEMP VOLTAGE TO °C

Definition of Cell Balancing

Cell balancing is defined as the application of differential currents to individual cells (or combinations of cells) in a series string. Normally, of course, cells in a series string receive identical currents. A battery pack requires additional components and circuitry to achieve cell balancing. For the ISL94208, the only external components required are balancing resistors.

Battery pack cells are balanced when all the cells in the battery pack meet two conditions.

1. If all cells have the same capacity, then they are balanced when they have the same relative State of Charge (SOC.) In this case, the Open Circuit Voltage (OCV) is a good measure of the SOC. If, in an out of balance pack, all cells can be differentially charged to full capacity (balanced), then they will subsequently cycle normally without any additional adjustments. This is mostly a one shot fix.
2. If the cells have different capacities, they are also considered balanced when the SOC is the same. But, since SOC is a relative measure, the absolute amount of capacity for each cell is different. To keep the cells with different capacities at the same SOC, cell balancing must provide differential amounts of current to cells in the series string during both charge and discharge on every cycle.

In an unbalanced battery pack, during charging, one or more cells will reach the maximum charge level before the rest of the cells in the series string. During discharge the cells that are not fully charged will be depleted before the other cells in the string, causing early undervoltage shutdown of the pack. These early charge and discharge limits reduce the usable charge in the battery.

Manufactured cell capacities are usually matched within 3%. If less than optimal Li-ion cells are introduced in to a series string pack or cells have been on the shelf for a long period prior to pack assembly, a 150mV difference at full charge is possible. This could result in a 13% to 18% reduction in battery pack capacity.

Soft-shorts

Soft-shorts are the primary cause of cell imbalance in Li-ion cells. Due to tiny imperfections in cell construction the cell can have very high resistance shorts on the order of 40,000Ω or more. The self discharge rate due to this higher resistance is on the order of 0.1mA or 3% per month. Most cells do not have this condition and can hold much of their capacity for years. Some cells which meet specifications when they leave the factory may sometimes exhibit this condition later. This is strictly an electromechanical condition. Used in a single cell pack, this cell can just be recharged and shows no capacity loss. But, in a series pack, a

cell with soft sorts could lose 3% per month, while another cell loses none at all. See Example 5.

Example 5: Cell balancing benefits.

Assume a 2 cell pack.
Assume cell 1 discharges 3%/month.
Assume cell 2 has negligible discharge.
Assume the cells start at the same 40% state of charge (SOC)
Assume the pack remains on the shelf for 3 months between charging, then it is charged, discharged and charged again before again being placed on the shelf.

Compare the pack performance with and without balancing:

Results without balancing:
At 3 months: Cell1=31% SOC, Cell2 = 40% SOC
After charge cycle: Cell1 = 91% SOC, Cell2 = 100%SOC
After discharge cycle: Cell1 = 0% SOC, Cell2 = 9% SOC
3 month pack capacity loss = 9%.
12 month pack capacity loss = 36%. A pack that had a 3 hour run time when new, lasts only 1.9 hours after one year

Results with balancing:
At 3 months: Cell1 = 31% SOC, Cell2 = 40% SOC
After charge cycle: Cell1 = 100% SOC, Cell2 = 100%SOC
After discharge cycle: Cell1 = 0% SOC, Cell2 =0% SOC

3 month pack capacity loss = 0%.
12 month pack capacity loss = 0%, with only minor, recoverable, loss if not used for a long period.

Cell Balance Operation

When choosing components for the cell balancing circuit, care is needed in the selection of the external current limiting resistor to keep the currents within reasonable limits. If balancing current is too high, power dissipation can be considerable - both internal to the IC and externally in the limiting resistor. The result can be battery pack heating or component stress. If balancing current is too low, balancing takes too long or requires too many charge/discharge cycles to return a benefit. The result is ineffective or non-existent cell balancing.

The microcontroller manages cell balancing by setting a bit in the Cell Balance Register. Each bit in the register corresponds to one cell's balancing control. With the bit set, an internal cell balancing FET turns on. This shorts an external resistor across the specified cell. The maximum current that can be drawn from (or bypassed around) the cell is 200mA, based on the ISL94208 limits. This current is set by selecting the value of the external resistor. Figure 40 shows an example with a 200mA (maximum) balancing current.

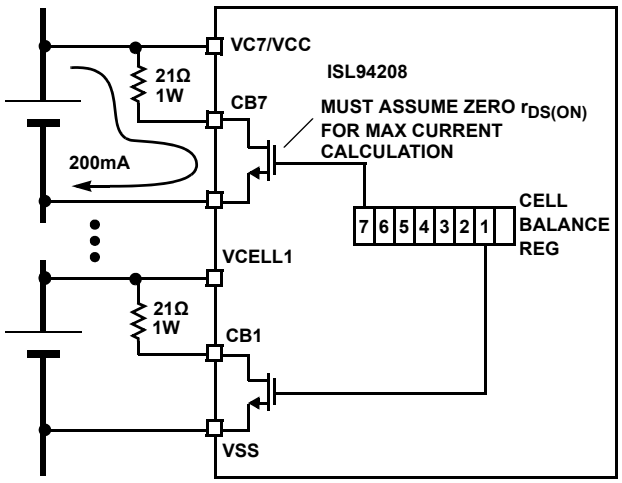


FIGURE 40. CELL BALANCING CONTROL EXAMPLE WITH 100mA BALANCING CURRENT

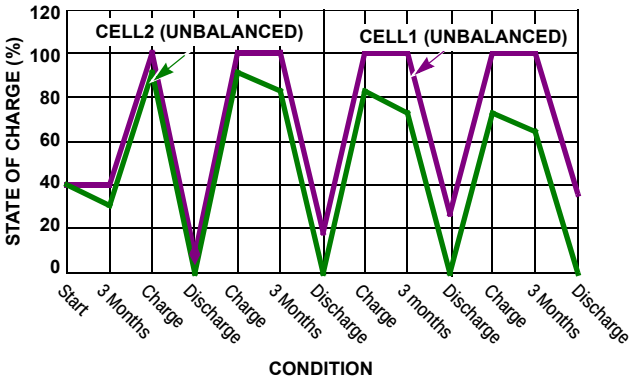


FIGURE 41. WITHOUT CELL BALANCING

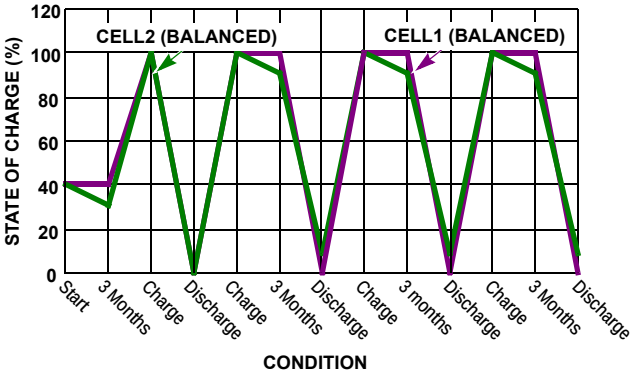


FIGURE 42. WITH CELL BALANCING

To program a balancing current of 200mA, start with a cell voltage of 4.2V and assume an internal resistance of 0Ω. This internal resistance is an ideal minimum $r_{DS(ON)}$. It will be non-zero, but to keep the maximum current at 200mA per cell, start by assuming this zero internal resistance. This balancing condition calls for an external resistor of 21Ω. With this value resistor, the external resistor dissipates 0.84W and the power dissipation inside the ISL94208 is zero. The external resistor should be sized to handle this power dissipation. (Ideally, to minimize heating, the goal is to use a 4W or greater resistor, but more realistically, because of board space and cost, the choice would be the use of a 2W resistor.)

Next, to make sure the device does not dissipate too much power through the internal FET, assume an external resistor of 21Ω and an internal FET resistance of 7Ω. This gives a balancing current of 150mA (4.2V/28Ω). The external resistor in this case dissipates 0.55W and the IC FET dissipates 158mW. The ISL94208 package has a power dissipation limit of 400mW. So, because of the heat generated internally from this aggressive balancing, there should be a software limit to balance only one or two cells at a time.

With lower balancing current, more balancing FETs can be turned on at once, without exceeding the device power dissipation limits or generating excessive balancing current. A reasonable compromise between aggressive balancing and power dissipation is a balancing current of about 100mA. A 42Ω/2W cell balancing resistor sets this maximum balancing current and has a maximum power dissipation of 420mW. The internal balancing FET has a maximum dissipation of 70mW, allowing four to five cell balancing FETs to be on at the same time.

The above calculations are for maximum cell voltages. But, as the cell voltage drops, the overall power dissipation also drops.

The ISL94208 supports battery packs with multiple cells in parallel. With more than 2 cells in parallel cell balancing becomes more difficult due to the higher pack capacities. At these higher capacities, the maximum 200mA balancing current limits the rate of balancing. To deal with this, an external P-Channel FET can be used to provide higher currents. Figure 43 shows an example of such a circuit. In this case it is even more important to separate the voltage monitoring and cell balancing paths to get accurate readings of the cell voltage while cell balancing is on. This connection of cell balancing components isolates the cell balancing from the cell monitoring, so monitoring and balancing can be performed simultaneously (although there may be some affect due to voltage drops on the connecting wires and in the cell voltage itself due to internal resistance.)

Another design consideration is to choose an external P-channel FET with a gate turn on voltage below the minimum cell voltage that balancing will take place. For example, if the cells will be balanced down to 2.5V, then the FET turn on voltage needs to be less than 2.5V. The circuit of Figure 43 provides up to 400mA of balancing current. This requires the use of 3 to 5W balancing resistors and 1W cell balancing transistors.

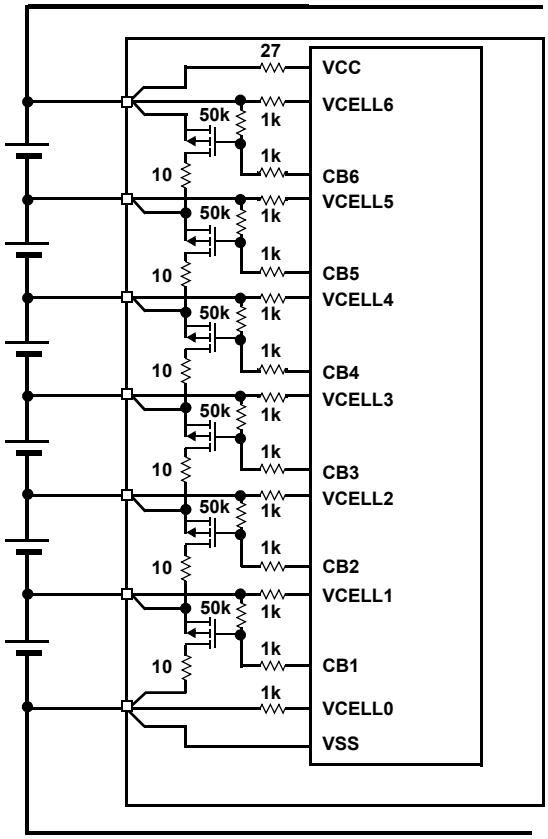


FIGURE 43. HIGH CURRENT CELL BALANCING CIRCUIT

Cell Balance Control Algorithm

Designing the software for cell balancing can become quite difficult as there are several limitations that should be considered and several difficult obstacles to overcome. Some of the design elements of a cell balancing algorithm are listed below:

1. **Maximum voltage differential between cells.** If the difference between the cells is too great, it could indicate that there is a bad cell. In this case, the decision by the microcontroller code might be to shut down the pack. Alternatively, it could turn off discharge, but allow charging in an attempt to rebalance the cells.
2. **Minimum voltage differential between cells.** If the cell voltage differential is too small, then it could be said the cells are already balanced. The decision about what voltage differential is too small is primarily based on the accuracy of the voltage measurement system. If the error in the measurement system is greater than the minimum cell balance differential, then a cell could be balanced that did not need to be, and the cell imbalance can increase.
3. **Temperature limits on balancing.** It is usually desirable to refrain from balancing when the cells are too hot or too cold. When cells are too hot, balancing them could increase the temperature of the cells. When cells are too cold charging should be restricted, limiting the opportunities for balancing.
4. **Maximum and minimum voltage on the individual cells being balanced.** This is not usually a problem and cells can be balanced all the way from the under charge level to the over charge level. However, if the balancing operation affects the

cell measurement, then operating the cell balancing algorithm at the capacity extremes may cause significant changes in the observed cell voltage, leading to pack shut down or resulting in the attempted balance of cells that do not need balancing. Also, as the cell voltages near their maximum, it is necessary to keep a close watch on the voltage, to avoid over charging the cells. It may not be possible to balance at the same time as when closely monitoring the cells near the over charge limit.

5. **Balancing on time vs. off time.** Ideally, there would not need to be a balancing on and off time. However, there are two benefits. First, using an on and off time allows management of the heat dissipated during balance. Second, without using external balancing FETs, any significant balancing current will affect the voltage at the ISL94208 VCELLn pin when the balancing is turned on. Adding a separate “Kelvin” connection from the terminal of the cell to the VCELLn pin (see Figure 1 and Figure 43), minimizing resistance in the cell to board connection, and balancing with less current all reduce the voltage measurement error. But, in general, the cell balance circuit must turn off periodically for the microcontroller to get a good reading of the cell voltages for managing the over charge and under charge condition of the cells as well as to determine the continuing need for cell balancing.

   The decision to balance a cell or not should be made before a balance cycle begins. Then, the balancing continues on the same cells for the duration of the on time. If any of the cells start the cycle as one of the “over charged” cells, but end as the least charged cell, then either the minimum voltage delta is too small or the balancing on time is too long.

6. **Maximum number of cells balanced at a time.** As mentioned earlier, the total number of cells balanced at any one time may be limited by the package power dissipation levels. This needs to be comprehended in the algorithm.

7. **Balancing order.** The algorithm normally sorts the cell voltages in order from high to low. Then, if the difference between any higher voltage cell and the minimum voltage cell exceeds the minimum balancing differential, then that cell balance FET is turned on. The algorithm starts by turning on the highest voltage cell, then the next highest, and so on until the maximum number of balanced cells is reached or no additional cells have a high enough voltage differential.

8. **Balance during charge or discharge or both.** Balancing cells during discharge conditions is not common. In this case charge from the pack is lost in the balancing resistors instead of the load during a period of time when maximum energy is required. Balancing during discharge reduces the pack capacity in the short term. It could be that this short term loss results in a long term gain, if the cells can be balanced quickly, but it is not obvious that this is the case.

   Balancing cells during the charge condition is the more common technique, since there is energy available from the charger to replenish that lost through the cell balance resistors. By balancing during charge, it is necessary to increase the charge current slightly to keep the overall charge time from increasing.

   The best method of implementing cell balancing during charge is to include a communication path between the pack microcontroller and the charger. This communication path allows the charger to monitor individual cell voltages, but it also allows the charger to let the pack know that a charger is present so balancing can commence. Alternatively, if the pack does not have a signal that there is a charger, then the pack needs to be able to detect the presence of a charger (or a load) in order to make a decision about balancing.

Current direction detection

For cell balancing or power management, if there is no charger communication path (as in a two terminal pack for example), the microcontroller code inside the pack needs to detect the presence of a charging or discharging current or use the pack voltage and cell voltages to determine if a charger or load is connected or not. This is not a trivial solution.

Additional hardware can be used to monitor the current direction and can even monitor current amplitude, but this external circuitry adds cost. This additional hardware may also have difficulty monitoring very low current.

An example of a low cost solution for detecting charge and discharge current is shown in Figure 44. In this circuit a dual P-channel FET is used to provide an offset to the op amp for the charge current detection. This is the most difficult condition, because the voltage goes negative relative to the microcontroller ground. In this case, the voltage on the non-inverting input to the op amp goes down as the charge current increases. The 1kΩ resistor provides some offset, so the positive terminal is normally higher than the negative terminal and the comparator output is high. This turns on the NPN transistor and the charge indicator is low. As the charge current increases, the voltage on the positive terminal decreases until the threshold is reached and the output turns off. This sets the charge indicator high. The microcontroller reads this input to detect the presence of charge current.

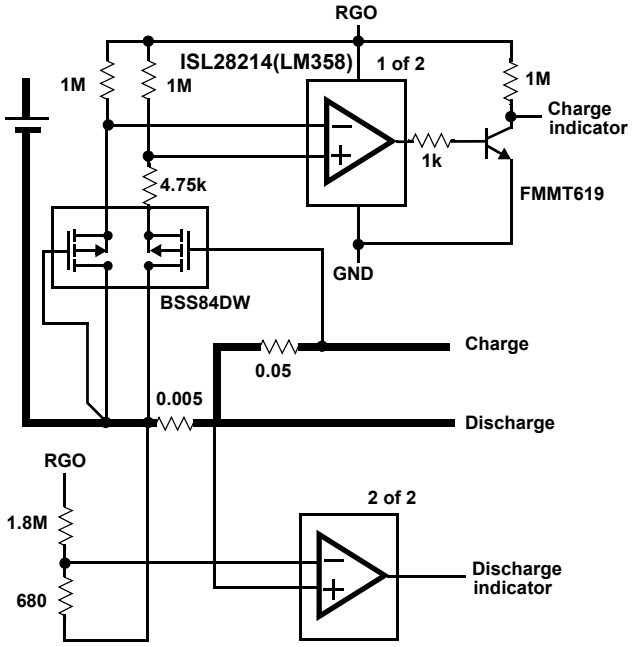


FIGURE 44. USING OP AMP AND FETS TO DETECT CHARGE AND DISCHARGE CURRENT

One of the problems with this circuit is the input offset of the op amp. If this offset is 2mV, then a current across the charge sense resistor could be as high as 36mA and not be detected. Using an op amp with lower offsets can allow detection of lower charge currents, but at higher cost.

In the circuit of Figure 44, the discharge current is detected with a simple comparator circuit. This can be simple, because the voltages are all positive. In this case, the 1.8M resistor and the 1k resistor set the offset of the op amp. As the discharge current increases, the voltage at the non-inverting terminal increases until the threshold is reached and the output turns on. This is monitored by the microcontroller.

There are two problems with this circuit. The first is the op amp input offset voltage. If the offset is higher than the applied reference offset, then the output will be active all the time. The specified values set an offset of about 2mV. Assuming no input offset, the minimum detectable discharge current is about 360mA.

The second problem with this circuit is that (with the LM358), the output does not swing all the way to the positive rail. Depending on the selection of the microcontroller, a high on the output of the LM358 may not be high enough to always register as a “1” with the microcontroller. The Intersil ISL28214 does not have this problem, the output does go rail to rail.

If an analog representation of the current is needed, the circuit of Figure 44 could be used by adding feedback to reduce the gain. Another alternative is the use of a voltage reference and a resistor divider. In the variation shown in Figure 45, the voltage on the input of the op amp is level shifted, so the output is always positive and, even though the Pack- pin goes negative with respect to ground, the inverting input to the op amp is always positive.

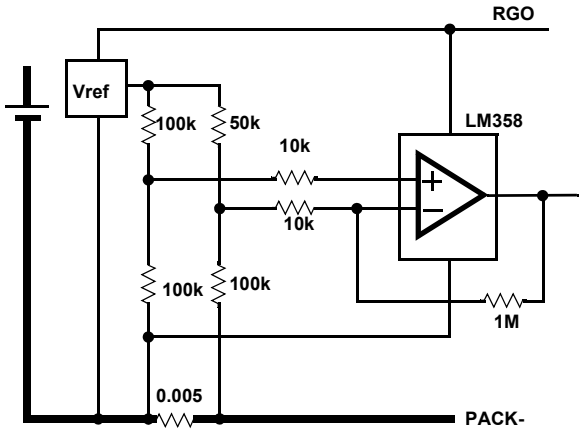
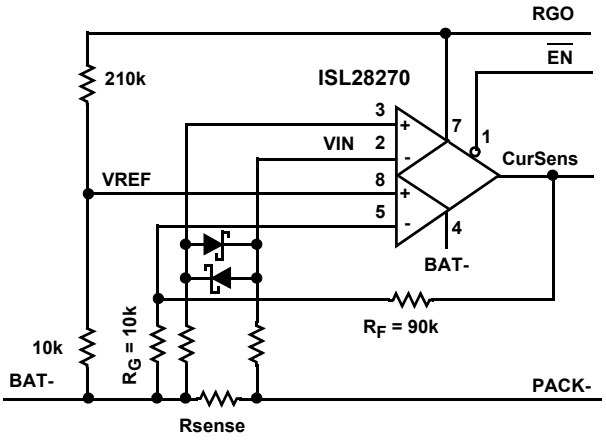


FIGURE 45. USING OP AMP AND VOLTAGE REFERENCE TO DETECT CHARGE/DISCHARGE CURRENT

For more performance, at a higher cost, an instrumentation amplifier can be used to get a current monitor output that provides a single signal that is referenced at half the RGO voltage. See Figure 46.

In both the solutions of Figures 45 and 46, there is additional software overhead to convert the analog current signal to a digital value. There is also additional test time to do a calibration on the circuit to determine the zero current output voltage. These circuits may also need some calibration at a higher current condition to adjust for any gain errors.



$$CurSens = \left(1 + \frac{R_F}{R_G}\right)(VIN) + \left(1 + \frac{R_F}{R_G}\right)(VREF)$$

$$CurSens = \left(1 + \frac{90k}{10k}\right)(VIN) + \left(1 + \frac{90k}{10k}\right)(VREF)$$

$$CurSens = (10 \times VIN) + 1.5V$$

FIGURE 46. SAMPLE CURRENT SENSE AMPLIFIER USING THE INTERSIL ISL28270

Without a direct hardware/software indication of current direction, a software only algorithm might make use the average dV/dt of the pack voltage to determine if the pack is charging or discharging. A pack being discharged generates a negative dV/dt. Charge current may also be detectable in this way, however, the pack can be far from the end of charge when the voltage reaches its constant voltage point. This may be acceptable for cell balance, if balancing is not desired at the very end of charge.

When using dV/dt measurements, the pack voltage may need to be filtered to avoid noise in the measurements and to smooth out short term variations in the load. The dV/dt value also needs to be averaged over a period of time, because in the middle of the cell voltage range there can be a lot of capacity change with very little corresponding voltage change. In this case, cell balancing could automatically stop if the dV/dt detection returns a zero charge rate.

Another problem with using the pack voltage for detecting a discharge condition is that it requires each cell voltage to be added together to get the pack voltage. When adding the individual cell voltages, the error and the noise on each input is also added. If there is an error of 5mV on each input, the pack voltage could show a total error of more than 35mV. This may not allow sufficient accuracy to detect charge current above the noise level.

An external circuit like the one shown in Figure 47 can be used to allow the microcontroller to directly monitor the pack voltage. The microcontroller turns on the circuit only during measurement to minimize current from the cells. The voltage at the output of this circuit is the pack voltage divided by 16. With the direct

measurement of the pack voltage, noise and variation in the measurement may be much less than simply adding the cell voltages and should allow detection of discharge current in software. The capacitor on the A/D input can help to reduce the noise, but the microcontroller will need to allow sufficient time for the voltage on the capacitor to settle prior to taking a measurement.

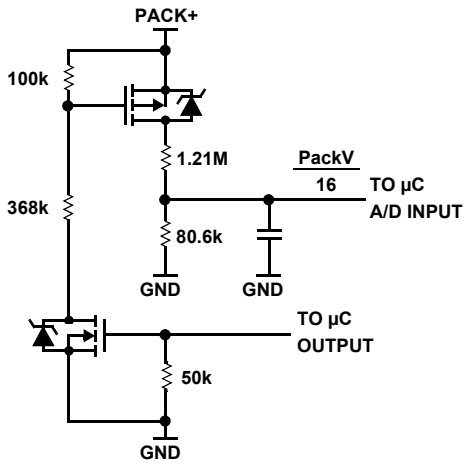


FIGURE 47. DIRECT MONITOR OF THE PACK VOLTAGE

The circuit in Figure 47 has another advantage. The software can monitor the sum of the cell voltages and compare them to the pack voltage from this circuit. If there is a large error, it could indicate some problem in the pack.

Pack Communications

If it is important to communicate with the pack microcontroller from the outside world, the easiest method is with a two wire interface such as the SMBus or I^2C bus. Most microcontrollers have one of these interfaces implemented in hardware. Alternatively, a one-wire interface could be developed, using microcontroller code.

Ground Referencing

Another design consideration for communication is that the microcontroller is ground referenced at the same point as the ISL94208. When the power FETs are off, this ground reference is different from the PACK negative terminal. So, communication between the pack and outside are only possible in the following conditions:

1. The power FETs are on. In this case, the PACK- terminal is roughly the same potential as the microcontroller ground.
2. The 2-wire external communication connector also provides the microcontroller ground voltage, so it is not necessary that the power FETs be on.

   CAUTION: In this case, the unit communicating with the pack cannot also use the PACK- terminal as a ground connection. The PACK- terminal should be floating. Otherwise, when the power FETs turn off, either an unsafe voltage differential occurs between the microcontroller ground and the PACK- pin, potentially damaging the microcontroller, or the monitoring device provides a discharge path around the power FETs. Neither condition is desired.

   Keep in mind also that a PC (for monitoring) and a power supply (for charging) may have their grounds connected together through their chassis and the AC power connection. The same is true if a scope is connected to the board. This may not be obvious. So using both of these units in the second configuration may require extra attention.

If monitoring of the pack is desired in production, then option 2 is normally sufficient. If a charger needs to communicate with the pack, then option 1 is required and the pack microcontroller needs to turn on the power FETs before communication is possible. Then, if the pack shuts down because of an over charge condition, the over charge condition must be resolved before communication is re-established.

Communication Port Reset

If, during a communication between the microcontroller and the ISL94208, the microcontroller stops communication due to a reset condition or noise, there is the possibility that the communication port can hang up. This happens if the ISL94208 is outputting a “0” on the SDA line when the microcontroller stops communication. In this state, the ISL94208 is awaiting a response from the microcontroller and the microcontroller is waiting for the SDA line to be released. To resolve this “stand-off”, use the following procedure before initial communication with the ISL94208 following a reset.

1. Examine the SCL and SDA pins
2. If SCL is high and SDA is low, perform steps 3 through 6 repeatedly to a maximum 9 times. After 9 loops of steps 3 through 6, if SDA is still stuck low, then this is an unrecoverable bus error.
3. Assert SCL low
4. Pause a few ms
5. Assert SCL high
6. Examine SDA. If it is now high, break out of the loop, and continue normal operation.
7. (Normal Operation) – Assert I2C START condition, etc.

Other Hardware Design Information

Packs with More than 7-Series Connected Cells

For applications that require more than 6-series connected cells, look at the ISL94212 .

Device Reset

The ISL94208 does not have a reset and a reset is not normally needed. However, if an external reset is desired, to clear any unknown condition with the part, the circuit of Figure 48 is suggested. This circuit, when activated by the microcontroller, pulls the VBACK input below the minimum POR voltage of about 1.5V, but not below about 0.9V. (Note: Pulling VBACK down to 0V also generates a reset, but the reset happens only when VBACK is released. This generates a short pulse on RGO, but the

duration of the RGO off period is based on the rise time of the VBACK input, so it requires an additional capacitor to control the RGO off duration.)

This circuit requires a series input resistor on VBACK and the microcontroller needs to hold the FET on long enough to force a reset (see Figure 49) and the time depends on the RGO capacitor and current.

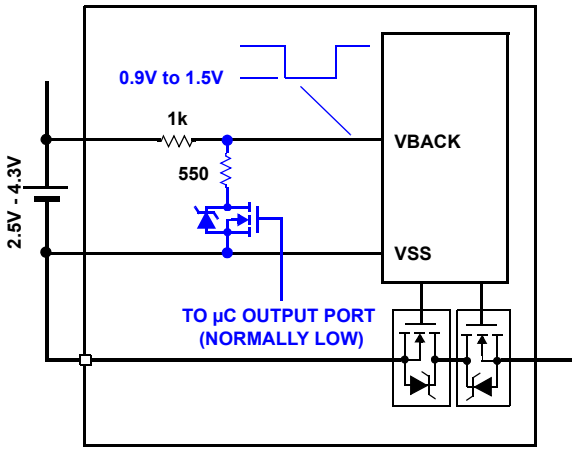


FIGURE 48. DIAGRAM OF EXTERNAL RESET CIRCUIT

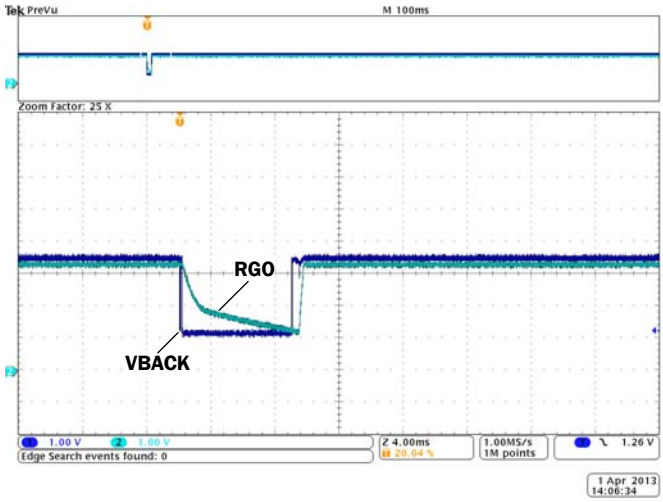


FIGURE 49. VBACK RESET PULSE

Power-Up Considerations

- When connecting the cells sequentially (from the bottom up,) there may be enough voltage on VBAT to power the RGO regulator when only a few cells are connected. If so, then the microcontroller is powered and the microcode starts running. If the microcontroller has code that puts the pack to sleep when a cell voltage is too low, then the pack could go to sleep immediately on initial partial connection of the cells.

There are several ways to avoid this initial power down.

- Connect all cells fast enough to have all connections made prior to the RGO powering the microcontroller. This likely requires the use of a connector on the board and not soldering individual wires.
- Provide software code that waits a while before shutting down in response to a low cell voltage.

Production Board Testing

When using an automated tester to test the ISL94208 board it is important to make sure that the power supply turn on is clean and does not stress the part. This means that there should be no over voltage spikes (ringing) and that there are no negative voltage spikes.

Figure 50 shows a negative 5V spike on VCELL1 with an input current of 10mA. Since, in this case, the PCB had a 1k series resistor on VCELL1 and on VBACK (both connect to the CELL1 of the tester), a negative 5V would have generated 5mA on each lead. The 10mA measured current indicates that the input resistors provided a limit to the current. If the PCB had used smaller input resistors, the current pulse and voltage spike would have been higher.

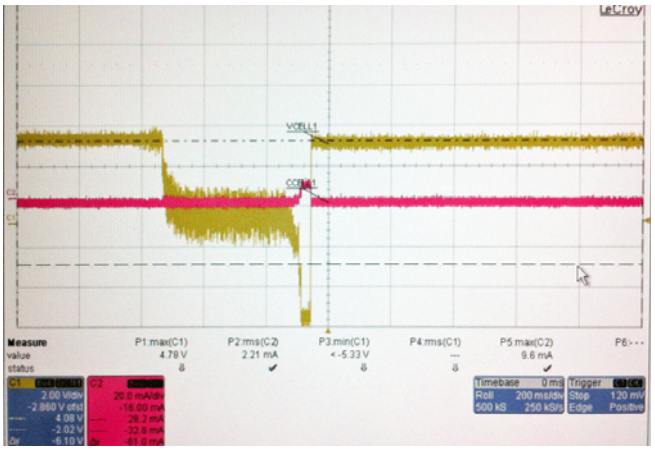


FIGURE 50. ISL94208 TESTER NEGATIVE VOLTAGE SPIKE

While the negative pulse in Figure 50 is not likely to damage the ISL94208, it is not a desired test condition and it would certainly be worse with smaller value input resistors. The tester hardware and software should be designed to avoid these conditions.

The best way to design the tester software is to:

- Whenever voltage is applied to and removed from the part it should be ramped up and ramped down (this can be done in multiple steps.)
- If there is a relay in the power path, switch it only when the voltage across the relay contacts is 0V.
- Avoid plugging the board into a socket that already has power applied, since it is difficult to control the connection sequence and the voltages/current applied to the board.